

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild μA741**

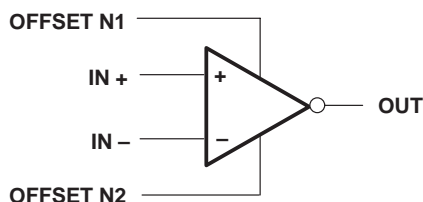
description

The μA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

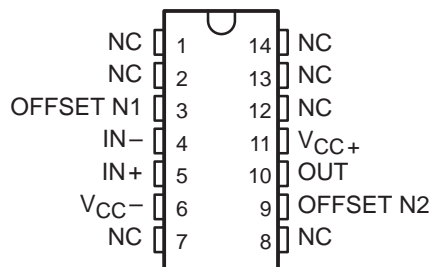
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The μA741C is characterized for operation from 0°C to 70°C. The μA741I is characterized for operation from -40°C to 85°C. The μA741M is characterized for operation over the full military temperature range of -55°C to 125°C.

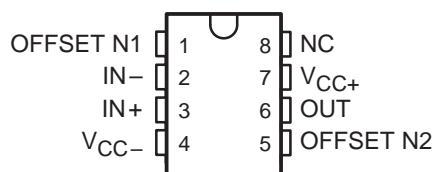
symbol



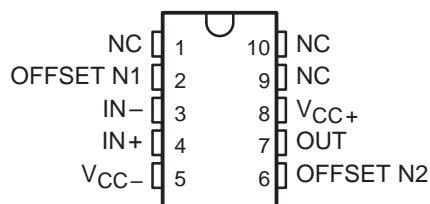
μA741M . . . J PACKAGE
(TOP VIEW)



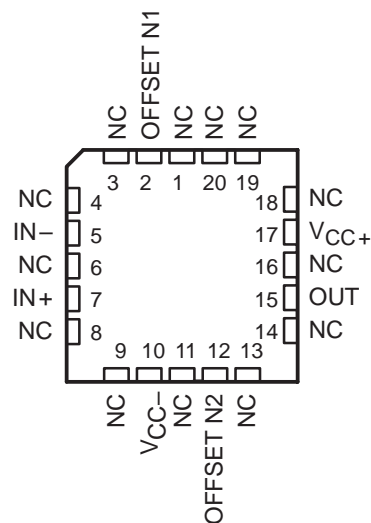
μA741M . . . JG PACKAGE
μA741C, μA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



μA741M . . . U PACKAGE
(TOP VIEW)



μA741M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

μA741, μA741Y GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

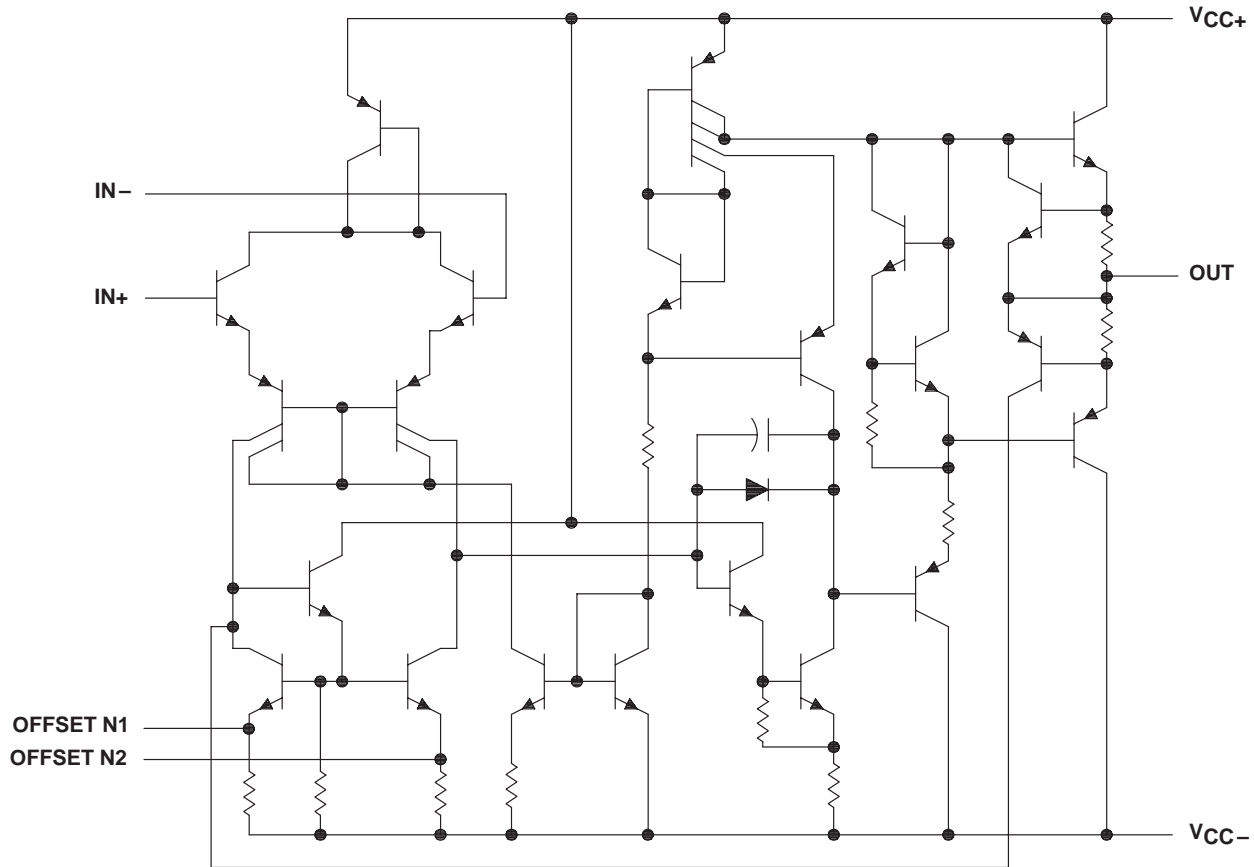
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AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | | | | | CHIP FORM (Y) |
|----------------|-------------------|-------------------|-----------------|------------------|-----------------|------------|---------------|---------------|
| | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (J) | CERAMIC DIP (JG) | PLASTIC DIP (P) | TSSOP (PW) | FLAT PACK (U) | |
| 0°C to 70°C | μA741CD | | | | μA741CP | μA741CPW | | μA741Y |
| -40°C to 85°C | μA741ID | | | | μA741IP | | | |
| -55°C to 125°C | | μA741MFK | μA741MJ | μA741MJG | | | μA741MU | |

The D package is available taped and reeled. Add the suffix R (e.g., μA741CDR).

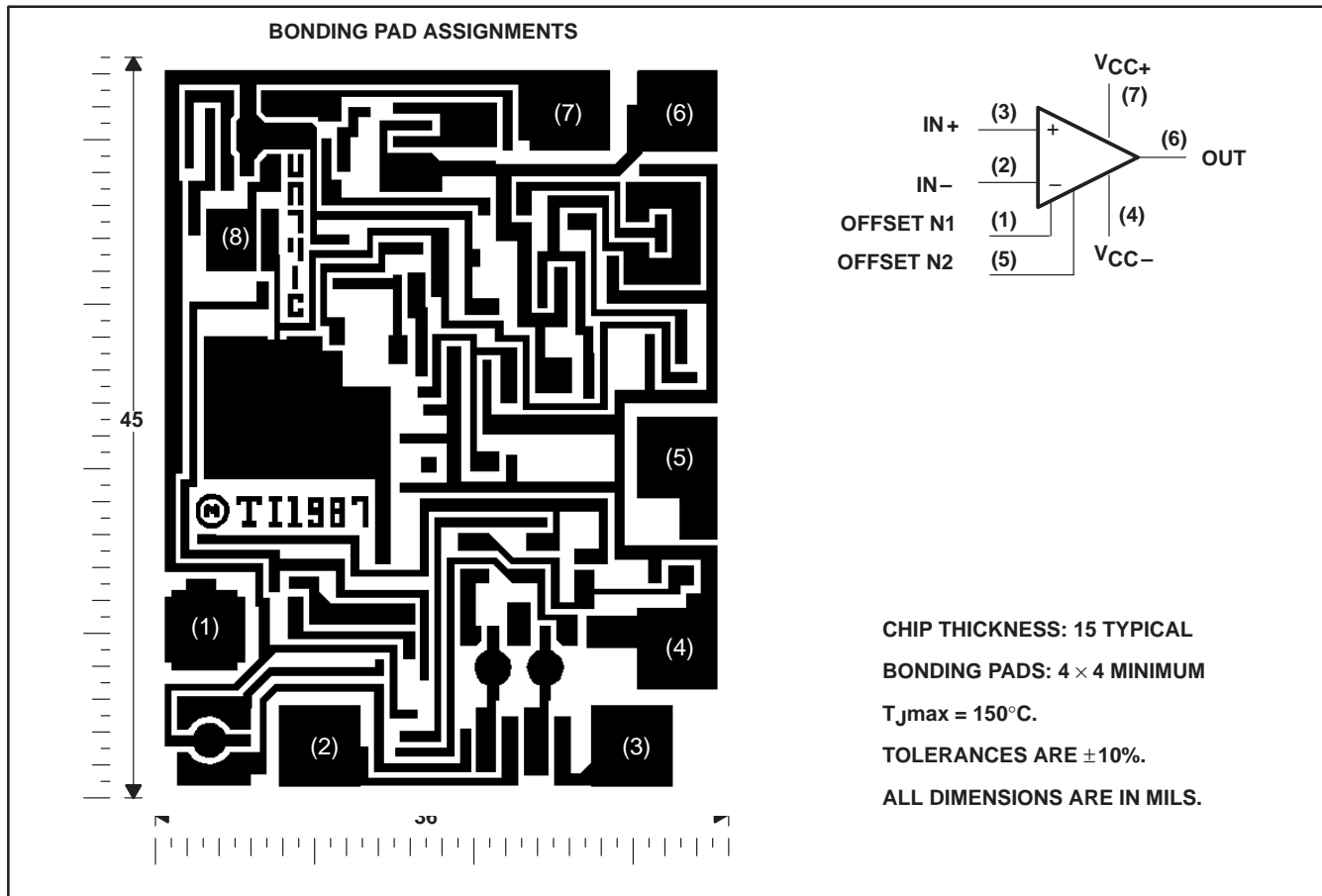
schematic



| Component Count | |
|-----------------|----|
| Transistors | 22 |
| Resistors | 11 |
| Diode | 1 |
| Capacitor | 1 |

μA741Y chip information

This chip, when properly assembled, displays characteristics similar to the μA741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



μ A741, μ A741Y GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | μ A741C | μ A741I | μ A741M | UNIT |
|---|------------------------------|-------------|-------------|--------------|
| Supply voltage, V_{CC+} (see Note 1) | 18 | 22 | 22 | V |
| Supply voltage, V_{CC-} (see Note 1) | -18 | -22 | -22 | V |
| Differential input voltage, V_{ID} (see Note 2) | ± 15 | ± 30 | ± 30 | V |
| Input voltage, V_I any input (see Notes 1 and 3) | ± 15 | ± 15 | ± 15 | V |
| Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-} | ± 15 | ± 0.5 | ± 0.5 | V |
| Duration of output short circuit (see Note 4) | unlimited | unlimited | unlimited | |
| Continuous total power dissipation | See Dissipation Rating Table | | | |
| Operating free-air temperature range, T_A | 0 to 70 | -40 to 85 | -55 to 125 | $^{\circ}$ C |
| Storage temperature range | -65 to 150 | -65 to 150 | -65 to 150 | $^{\circ}$ C |
| Case temperature for 60 seconds | FK package | | 260 | $^{\circ}$ C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | J, JG, or U package | | 300 | $^{\circ}$ C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D, P, or PW package | | 260 | $^{\circ}$ C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to ground or either power supply. For the μ A741M only, the unlimited duration of the short circuit applies at (or below) 125 $^{\circ}$ C case temperature or 75 $^{\circ}$ C free-air temperature.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^{\circ}$ C POWER RATING | DERATING FACTOR | DERATE ABOVE T_A | $T_A = 70^{\circ}$ C POWER RATING | $T_A = 85^{\circ}$ C POWER RATING | $T_A = 125^{\circ}$ C POWER RATING |
|---------|---|-----------------------|-----------------------|--------------------------------------|--------------------------------------|---------------------------------------|
| D | 500 mW | 5.8 mW/ $^{\circ}$ C | 64 $^{\circ}$ C | 464 mW | 377 mW | N/A |
| FK | 500 mW | 11.0 mW/ $^{\circ}$ C | 105 $^{\circ}$ C | 500 mW | 500 mW | 275 mW |
| J | 500 mW | 11.0 mW/ $^{\circ}$ C | 105 $^{\circ}$ C | 500 mW | 500 mW | 275 mW |
| JG | 500 mW | 8.4 mW/ $^{\circ}$ C | 90 $^{\circ}$ C | 500 mW | 500 mW | 210 mW |
| P | 500 mW | N/A | N/A | 500 mW | 500 mW | N/A |
| PW | 525 mW | 4.2 mW/ $^{\circ}$ C | 25 $^{\circ}$ C | 336 mW | N/A | N/A |
| U | 500 mW | 5.4 mW/ $^{\circ}$ C | 57 $^{\circ}$ C | 432 mW | 351 mW | 135 mW |



μA741, μA741Y
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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | μA741C | | | μA741I, μA741M | | | UNIT |
|--|----------------------------------|------------|--------|-----|-----|----------------|-----|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IO} Input offset voltage | $V_O = 0$ | 25°C | | 1 | 6 | | 1 | 5 | mV |
| | | Full range | | | 7.5 | | | 6 | |
| $\Delta V_{IO(adj)}$ Offset voltage adjust range | $V_O = 0$ | 25°C | | ±15 | | | ±15 | | mV |
| I_{IO} Input offset current | $V_O = 0$ | 25°C | | 20 | 200 | | 20 | 200 | nA |
| | | Full range | | | 300 | | | 500 | |
| I_{IB} Input bias current | $V_O = 0$ | 25°C | | 80 | 500 | | 80 | 500 | nA |
| | | Full range | | | 800 | | | 1500 | |
| V_{ICR} Common-mode input voltage range | | 25°C | | ±12 | ±13 | | ±12 | ±13 | V |
| | | Full range | | | ±12 | | | ±12 | |
| V_{OM} Maximum peak output voltage swing | $R_L = 10$ kΩ | 25°C | | ±12 | ±14 | | ±12 | ±14 | V |
| | $R_L \geq 10$ kΩ | Full range | | | ±12 | | | ±12 | |
| | $R_L = 2$ kΩ | 25°C | | ±10 | ±13 | | ±10 | ±13 | |
| | $R_L \geq 2$ kΩ | Full range | | | ±10 | | | ±10 | |
| A_{VD} Large-signal differential voltage amplification | $R_L \geq 2$ kΩ | 25°C | | 20 | 200 | | 50 | 200 | V/mV |
| | $V_O = \pm 10$ V | Full range | | | 15 | | | 25 | |
| r_i Input resistance | | 25°C | | 0.3 | 2 | | 0.3 | 2 | MΩ |
| r_o Output resistance | $V_O = 0$, See Note 5 | 25°C | | | 75 | | | 75 | Ω |
| C_i Input capacitance | | 25°C | | | 1.4 | | | 1.4 | pF |
| CMRR Common-mode rejection ratio | $V_{IC} = V_{ICRmin}$ | 25°C | | 70 | 90 | | 70 | 90 | dB |
| | | Full range | | | 70 | | | 70 | |
| k_{SVS} Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) | $V_{CC} = \pm 9$ V to ± 15 V | 25°C | | 30 | 150 | | 30 | 150 | μV/V |
| | | Full range | | | 150 | | | 150 | |
| I_{OS} Short-circuit output current | | 25°C | | ±25 | ±40 | | ±25 | ±40 | mA |
| I_{CC} Supply current | $V_O = 0$, No load | 25°C | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| | | Full range | | | 3.3 | | | 3.3 | |
| P_D Total power dissipation | $V_O = 0$, No load | 25°C | | 50 | 85 | | 50 | 85 | mW |
| | | Full range | | | 100 | | | 100 | |

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the μA741C is 0°C to 70°C, the μA741I is -40°C to 85°C, and the μA741M is -55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ$ C

| PARAMETER | TEST CONDITIONS | μA741C | | | μA741I, μA741M | | | UNIT |
|----------------------------|---|--------|-----|-----|----------------|-----|-----|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t_r Rise time | $V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1 | | 0.3 | | | 0.3 | | μs |
| Overshoot factor | | | | 5% | | | 5% | |
| SR Slew rate at unity gain | $V_I = 10$ V, $C_L = 100$ pF, $R_L = 2$ kΩ, See Figure 1 | | 0.5 | | | 0.5 | | V/μs |



μ A741, μ A741Y GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | μ A741Y | | | UNIT |
|-----------------------------|--|----------------------------------|-------------|----------|-----|-----------------|
| | | | MIN | TYP | MAX | |
| V_{IO} | Input offset voltage | $V_O = 0$ | | 1 | 6 | mV |
| $\Delta V_{IO(\text{adj})}$ | Offset voltage adjust range | $V_O = 0$ | | ± 15 | | mV |
| I_{IO} | Input offset current | $V_O = 0$ | | 20 | 200 | nA |
| I_{IB} | Input bias current | $V_O = 0$ | | 80 | 500 | nA |
| V_{ICR} | Common-mode input voltage range | | ± 12 | ± 13 | | V |
| V_{OM} | Maximum peak output voltage swing | $R_L = 10$ k Ω | ± 12 | ± 14 | | V |
| | | $R_L = 2$ k Ω | ± 10 | ± 13 | | |
| A_{VD} | Large-signal differential voltage amplification | $R_L \geq 2$ k Ω | 20 | 200 | | V/mV |
| r_i | Input resistance | | 0.3 | 2 | | M Ω |
| r_o | Output resistance | $V_O = 0$, See Note 5 | | 75 | | Ω |
| C_i | Input capacitance | | | 1.4 | | pF |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR\text{min}}$ | 70 | 90 | | dB |
| k_{SVS} | Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) | $V_{CC} = \pm 9$ V to ± 15 V | | 30 | 150 | $\mu\text{V/V}$ |
| I_{OS} | Short-circuit output current | | ± 25 | ± 40 | | mA |
| I_{CC} | Supply current | $V_O = 0$, No load | | 1.7 | 2.8 | mA |
| P_D | Total power dissipation | $V_O = 0$, No load | | 50 | 85 | mW |

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | μ A741Y | | | UNIT |
|-----------|-------------------------|---|-------------|-----|-----|------------------|
| | | | MIN | TYP | MAX | |
| t_r | Rise time | $V_I = 20$ mV, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1 | | 0.3 | | μs |
| | Overshoot factor | | | 5% | | |
| SR | Slew rate at unity gain | $V_I = 10$ V, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1 | | 0.5 | | V/ μs |



PARAMETER MEASUREMENT INFORMATION

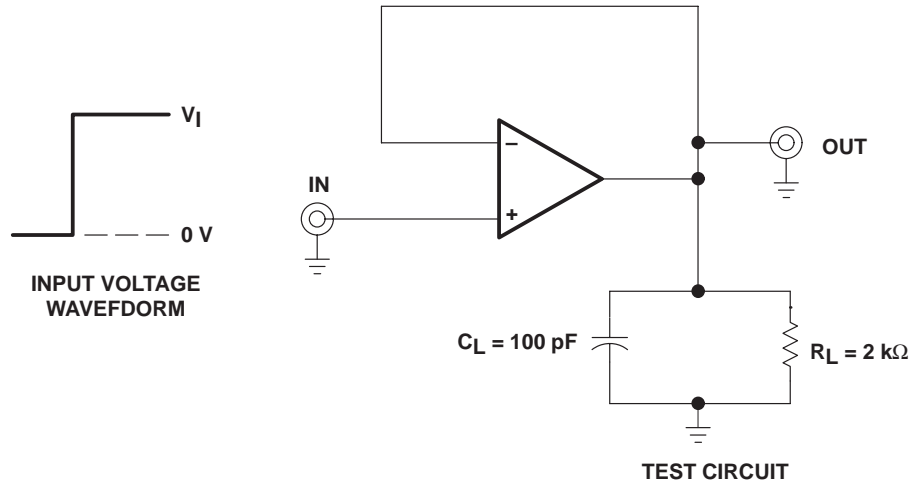


Figure 1. Rise Time, Overshoot, and Slew Rate

APPLICATION INFORMATION

Figure 2 shows a diagram for an input offset voltage null circuit.

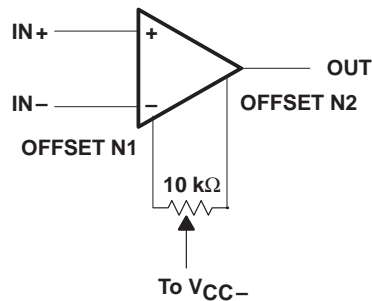


Figure 2. Input Offset Voltage Null Circuit

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TYPICAL CHARACTERISTICS†

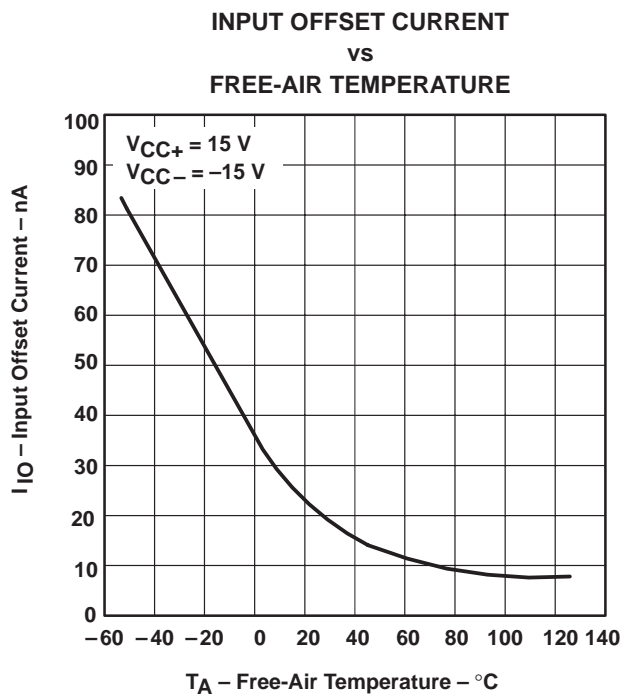


Figure 3

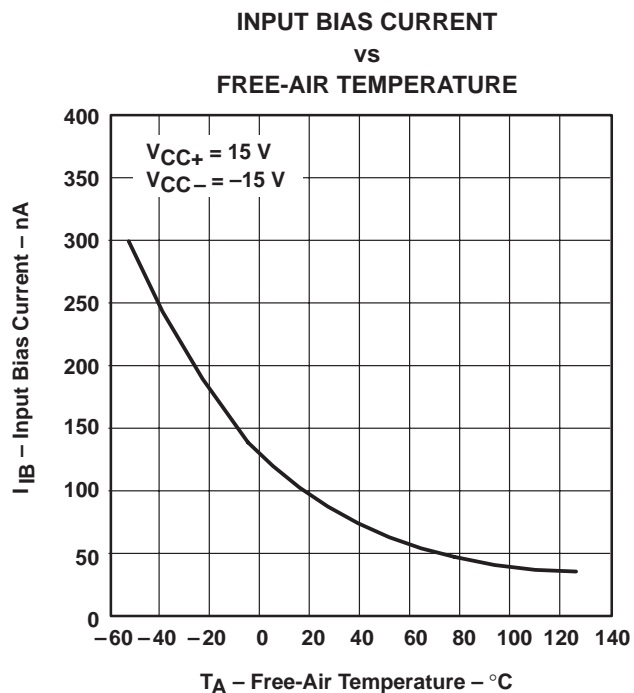


Figure 4

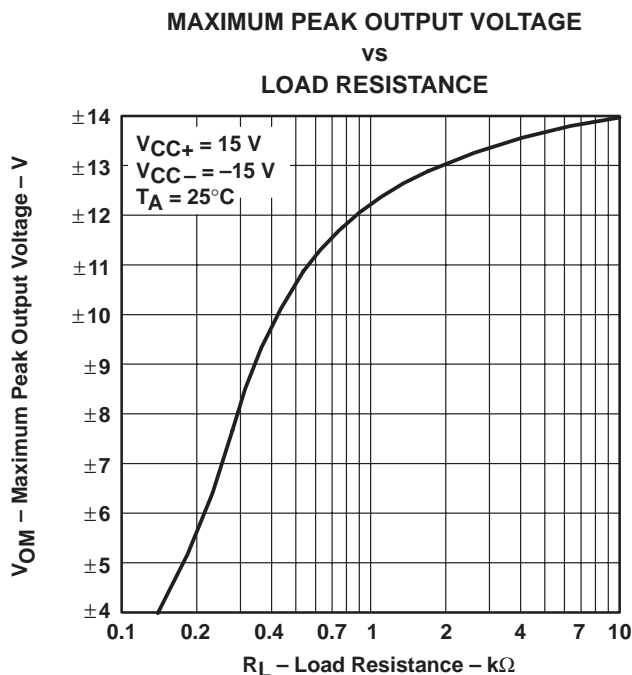


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

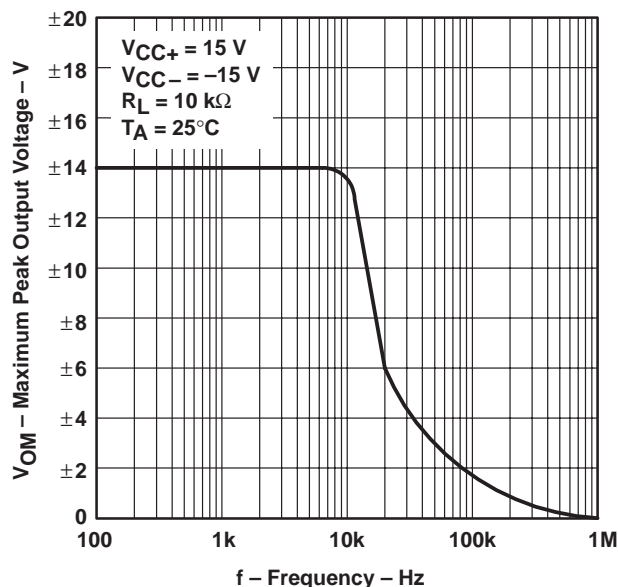


Figure 6

**OPEN-LOOP SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE**

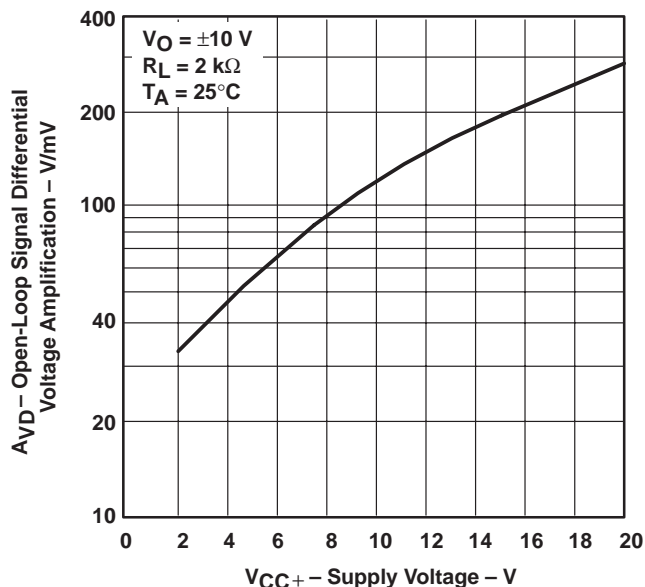
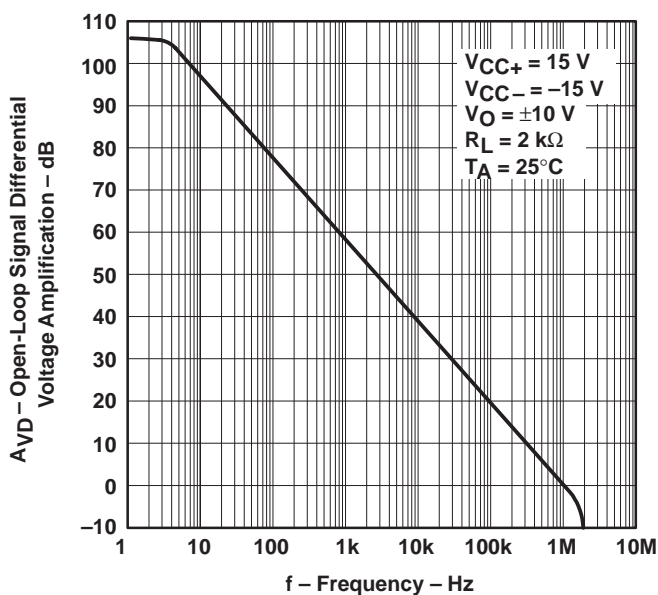


Figure 7

**OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY**



TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
VS
FREQUENCY

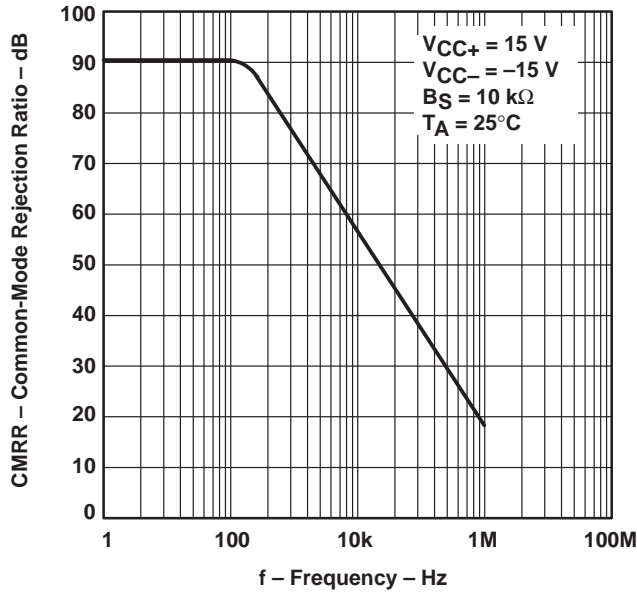


Figure 8

OUTPUT VOLTAGE
VS
ELAPSED TIME

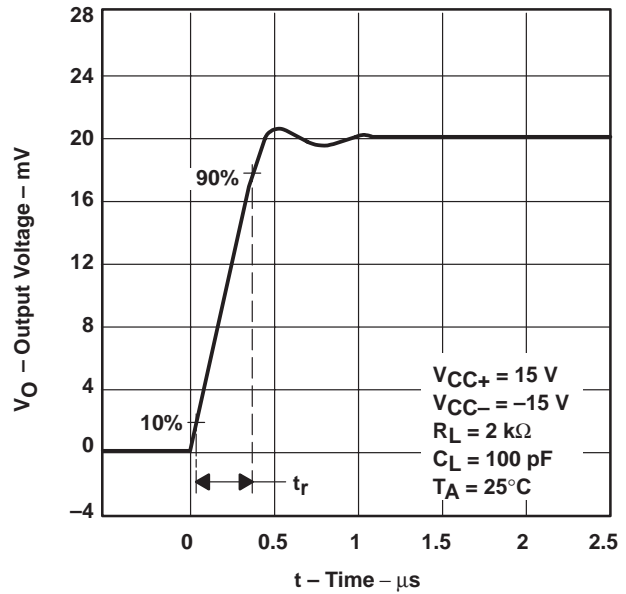


Figure 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

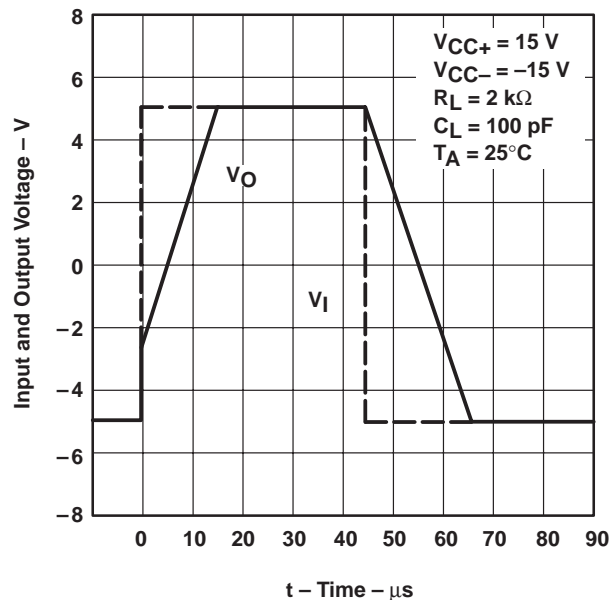


Figure 10

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| UA741CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CJG | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| UA741CJG4 | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| UA741CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| UA741CPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| UA741CPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CPSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741CPSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| UA741MFKB | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI |
| UA741MJ | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| UA741MJB | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| UA741MJG | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| UA741MJGB | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

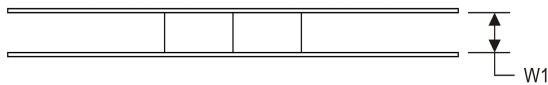
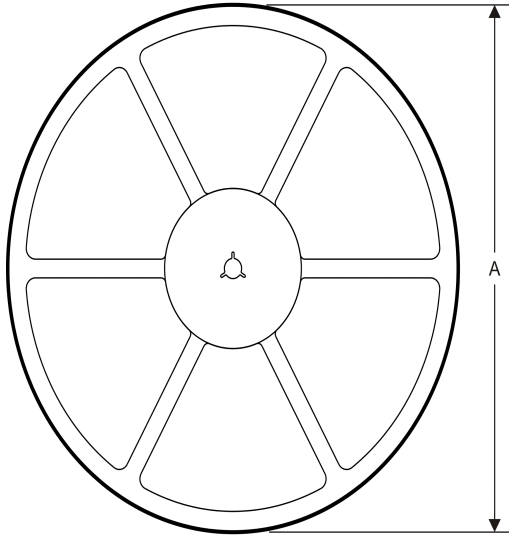
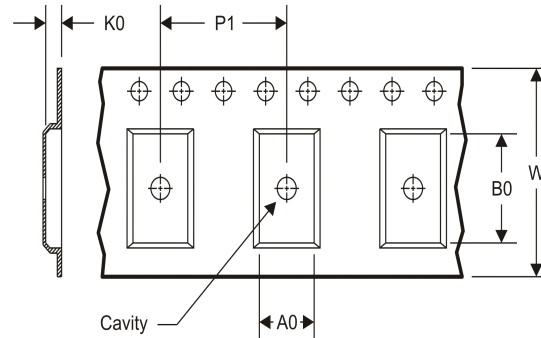
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UA741CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UA741CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

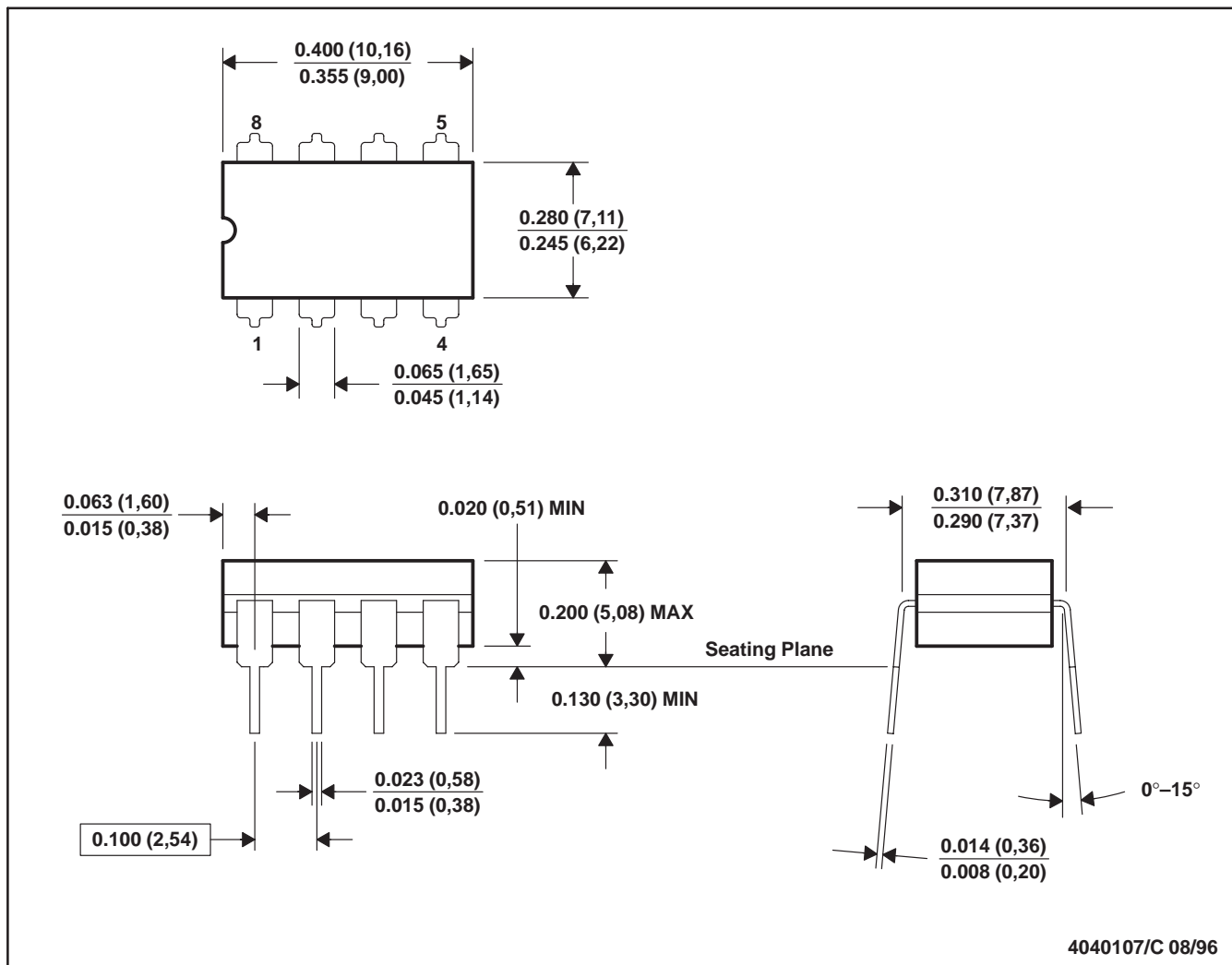


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| UA741CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| UA741CPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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