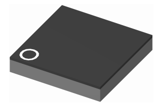
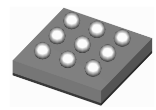




2.75-W FIXED GAIN MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **Maximize Battery Life and Minimize Heat**
  - **– 0.5-µA Shutdown Current**
  - **– 3.0-mA Quiescent Current**
  - **– High Efficiency Class-D**
    - **88% at 400mW at 8Ω**
    - **80% at 100mW at 8Ω**
- **Three Fixed Gain Versions**
  - **– TPA2032D1 has a gain of 2 V/V (6dB)**
  - **– TPA2033D1 has a gain of 3 V/V (9.5dB)**
  - **– TPA2034D1 has a gain of 4 V/V (12dB)**
- **Only One External Component Required**
  - **– Internal Matched Input Gain and Feedback Resistors for Excellent PSRR and CMRR**
  - **– Optimized PWM Output Stage Eliminates LC Output Filter**
  - **– PSRR (–75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Dedicated Voltage Regulator**
  - **– Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor**
  - **– CMRR (–69 dB)Eliminates Two Input Coupling Capacitors**
- **Thermal and Short-Circuit Protection**
- **Pinout Very Similar to TPA2010D1**
- **Wafer Chip Scale Packaging (WCSP)**
  - **– NanoFree™ Lead-Free (Pb-Free: YZF)**

APPLICATIONS

- **Ideal for Wireless Handsets, PDAs, and other mobile devices**

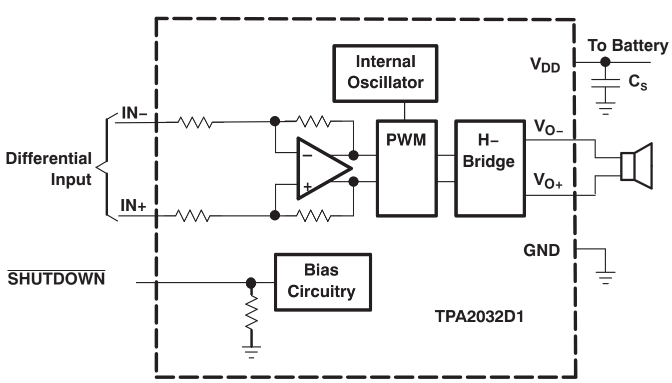
DESCRIPTION

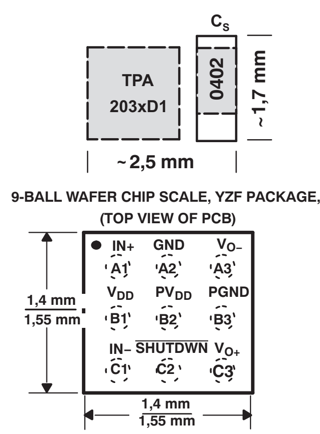
The TPA2032D1 (2V/V gain), TPA2033D1 (3V/V gain), and TPA2034D1 (4V/V gain) are 2.75-W high efficiency filter-free class-D audio power amplifiers, each in an approximately 1.5-mm × 1.5-mm wafer chip scale package (WCSP) that requires only one external component. The pinout is the same as the TPA2010D1 except that the external gain setting input resistors required by the TPA2010D1 are integrated into the fixed gain TPA203xD1 family.

Features like –75dB PSRR and improved RF-rectification immunity with a very small PCB footprint (WCSP amplifier plus single decoupling cap) make the TPA203xD1 family ideal for wireless handsets. A fast start-up time of 3.2 ms with minimal pop makes the TPA203xD1 family ideal for PDA applications.

In wireless handsets, the earpiece, speaker phone, and melody ringer can each be driven by a TPA203xD1. The TPA203xD1 family has a low 27-µV noise floor, A-weighted.

APPLICATION CIRCUIT





Note: Pin A1 is marked with a “0” .

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER	SYMBOL
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2032D1YZF [1]	BPX
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2033D1YZF [1]	BPY
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2034D1YZF [1]	BPZ

(1) The YZF package is only available taped and reeled. To order add the suffix *R* to the end of the part number for a reel of 3000, or add the suffix *T* to the end of the part number for a reel of 250 (e.g. TPA2032D1YZFR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

			TPA2032D1, TPA2033D1, TPA2034D1
V_{DD}	Supply voltage	In active mode	–0.3 V to 6 V
		In $\overline{\text{SHUTDOWN}}$ mode	–0.3 V to 7 V
V_I	Input voltage		–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature		–40°C to 85°C
T_J	Operating junction temperature		–40°C to 125°C
T_{stg}	Storage temperature		–65°C to 150°C
ESD	Electro-Static Discharge Tolerance - Human Body Model (HBM) for all pins[2]		2KV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The output pins Vo– and Vo+ are tolerant to 1.5KV HBM ESD

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.5		5.5	V
V_{IH}	High-level input voltage	$\overline{\text{SHUTDOWN}}$	1.3		V_{DD}	V
V_{IL}	Low-level input voltage	$\overline{\text{SHUTDOWN}}$	0		0.35	V
V_{IC}	Common mode input voltage range	V_{DD} = 2.5 V, 5.5 V	0.5		V_{DD}–0.8	V
T_A	Operating free-air temperature		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR (1 / θ_{JA})	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
YZF	4.8 mW/°C[1]	480 mW	264 mW	192 mW
YZF	7.5 mW/°C[2]	750 mW	412 mW	300 mW

(1) Derating factor measured with JEDEC Low-K board; 1S0P - One signal layer and zero plane layers.
(2) Derating factor measured with JEDEC High K board; 1S2P - One signal layer and two plane layers.
Please see JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information.
Please see JEDEC document page for downloadable copies: http://www.jedec.org/download/default.cfm.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	Inputs AC grounded, V_{DD} = 2.5 V to 5.5 V	TPA2032D1		5	25	mV
			TPA2033D1		5	25	
			TPA2034D1		5	25	
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V			–75	-61	dB
CMRR	Common mode rejection ratio	V_{IC} = 0.5 V to (V_{DD} –0.8 V)	V_{DD} = 2.5 V		–69	-52	dB
			V_{DD} = 3.6 V		– 69	-52	
			V_{DD} = 5.5 V		–69	-52	
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V				50	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = –0.3 V				5	µA
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load			4	5.7	mA
		V_{DD} = 3.6 V, no load			3		
		V_{DD} = 2.5 V, no load			2.2	3.7	
$I_{(SD)}$	Shutdown current	$V_{(\overline{SHUTDOWN})}$= 0.35 V, V_{DD} = 2.5 V to 5.5 V			0.5	0.8	µA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 2.5 V			550		mΩ
		V_{DD} = 3.6 V			420		
		V_{DD} = 5.0 V			350		
	Output impedance in $\overline{\text{SHUTDOWN}}$	$V_{(\overline{SHUTDOWN})}$ <= 0.35 V			2		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V		240	300	400	kHz
Gain		V_{DD} = 2.5 V to 5.5 V	TPA2032D1	5.5	6	6.5	dB
			TPA2033D1	9.0	9.5	10.0	
			TPA2034D1	11.5	12	12.5	
R_{PD}	Resistance of internal pulldown resistor from shutdown pin to GND				300		kΩ

OPERATING CHARACTERISTICS

T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	R_L = 4 Ω, THD + N = 10%, f = 1 kHz	V_{DD} = 5 V		2.75		W
			V_{DD} = 3.6 V		1.35		
			V_{DD} = 2.5 V		0.59		
		R_L = 4 Ω, THD + N = 1%, f = 1 kHz	V_{DD} = 5 V		2.25		W
			V_{DD} = 3.6 V		1.12		
			V_{DD} = 2.5 V		0.48		
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz	V_{DD} = 5 V		1.68		W
			V_{DD} = 3.6 V		0.85		
			V_{DD} = 2.5 V		0.38		
		R_L = 8 Ω, THD + N = 1%, f = 1 kHz	V_{DD} = 5 V		1.37		W
			V_{DD} = 3.6 V		0.68		
			V_{DD} = 2.5 V		0.31		
THD+ N	Total harmonic distortion plus noise	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω, f = 1 kHz			0.18%		
		V_{DD} = 3.6 V, P_O = 0.5 W, R_L = 8 Ω, f = 1 kHz			0.11%		
		V_{DD} = 2.5 V, P_O = 200 mW, R_L = 8 Ω, f = 1 kHz			0.10%		
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6 V, Inputs AC grounded with C_I = 1 µF	f = 217 Hz, $V_{(RIPPLE)}$ = 200 mV_{pp}		–73		dB
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω, A weighted noise			100		dB

OPERATING CHARACTERISTICS (continued)

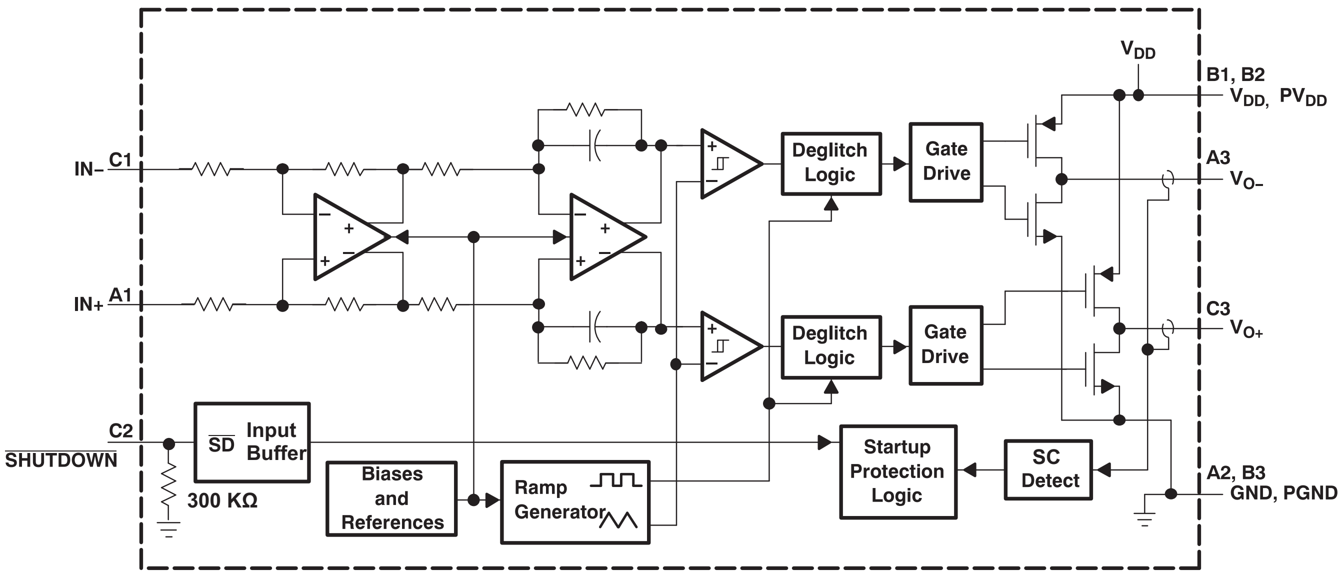
T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs AC grounded with C_i = 1 μF	No weighting		35		μV_{RMS}
			A weighting		27		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1.0 V_{pp} , V_{Cm} = 1.8 V	f = 217 Hz		–69		dB
R_I	Input impedance	A_V = 2 V/V			30.2		kΩ
		A_V = 3 V/V			22.8		
		A_V = 4 V/V			18.5		
	Start-up time from shutdown	V_{DD} = 3.6 V			3.2		ms

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	YZF		
IN–	C1	I	Negative differential audio input
IN+	A1	I	Positive differential audio input
V_{O-}	A3	O	Negative BTL audio output
V_{O+}	C3	O	Positive BTL audio output
GND	A2	I	Analog ground terminal. Must be connected to same potential as PGND using a direct connection to a single point ground.
PGND	B3		High-current Analog ground terminal. Must be connected to same potential as GND using a direct connection to a single point ground.
V_{DD}	B1	I	Power supply terminal. Must be connected to same power supply as PV_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
PV_{DD}	B2	I	High-current Power supply terminal. Must be connected to same power supply as V_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
$\overline{\text{SHUTDOWN}}$	C2	I	Shutdown terminal. When terminal is low the device is put into Shutdown mode.

FUNCTIONAL BLOCK DIAGRAM

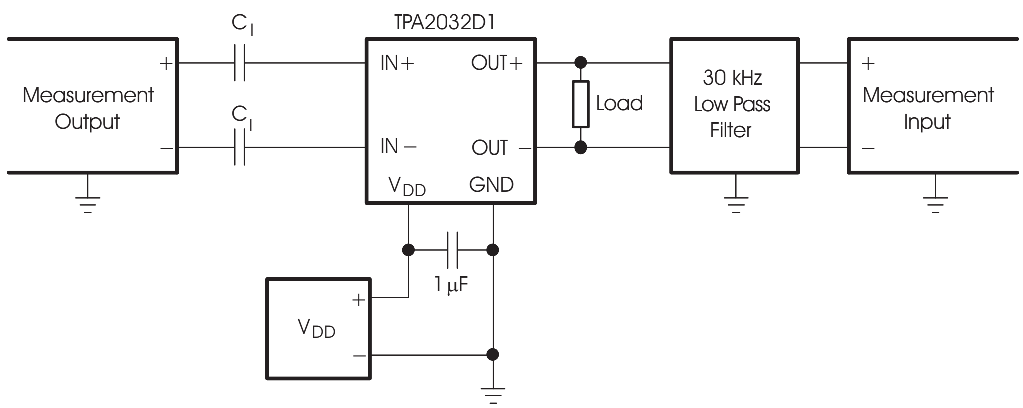


TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
	Efficiency	vs Output power	1, 2
P_D	Power dissipation	vs Output power	3, 4
	Supply current	vs Output power	5, 6
I_{DD}	Supply current	vs Supply voltage	7
$I_{(SD)}$	Shutdown current	vs Shutdown voltage	8
P_O	Output power	vs Load resistance	9, 10
		vs Supply voltage	11
THD+N	Total harmonic distortion plus noise	vs Output power	12, 13
		vs Frequency	14, 15, 16, 17
		vs Common-mode input voltage	18
K_{SVR}	Supply voltage rejection ratio	vs Frequency	19, 20, 21, 22, 23, 24, 25, 26, 27
	GSM power supply rejection	vs Time	28
		vs Frequency	29
K_{SVR}	Supply voltage rejection ratio	vs Common-mode input voltage	30, 31, 32
CMRR	Common-mode rejection ratio	vs Frequency	33
		vs Common-mode input voltage	34

TEST SET-UP FOR GRAPHS



(1) C_I was shorted for any common-mode input voltage measurement. All other measurements were taken with a 1-µF C_I (unless otherwise noted).

(2) A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30-kHz low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter (100Ω, 47-nF) is used on each output for the data sheet graphs.

EFFICIENCY vs OUTPUT POWER

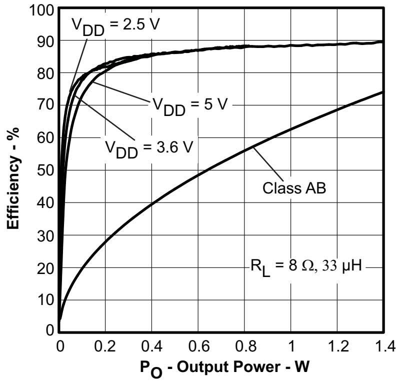


Figure 1.

EFFICIENCY vs OUTPUT POWER

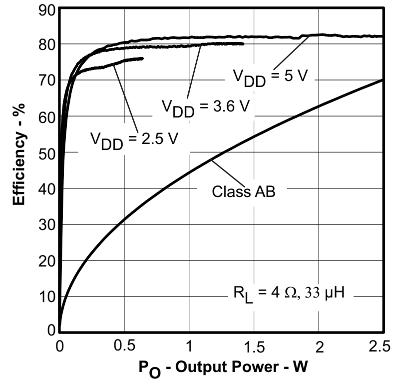


Figure 2.

POWER DISSIPATION vs OUTPUT POWER

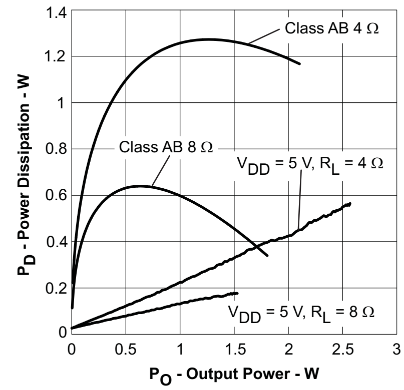


Figure 3.

POWER DISSIPATION vs OUTPUT POWER

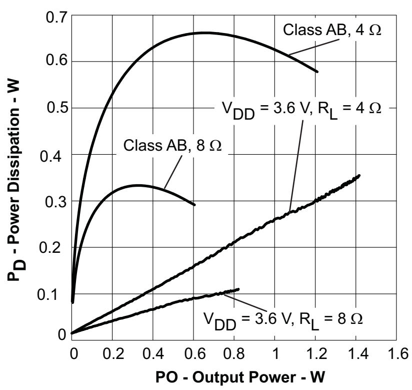


Figure 4.

SUPPLY CURRENT vs OUTPUT POWER

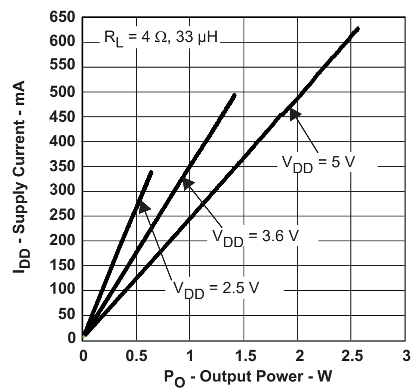


Figure 5.

SUPPLY CURRENT vs OUTPUT POWER

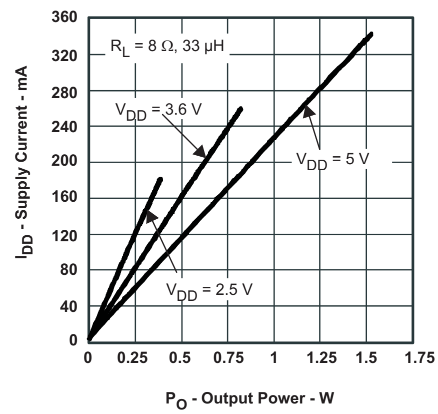


Figure 6.

SUPPLY CURRENT vs SUPPLY VOLTAGE

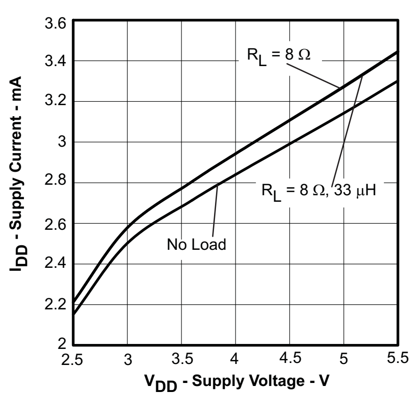


Figure 7.

SHUTDOWN CURRENT vs SHUTDOWN VOLTAGE

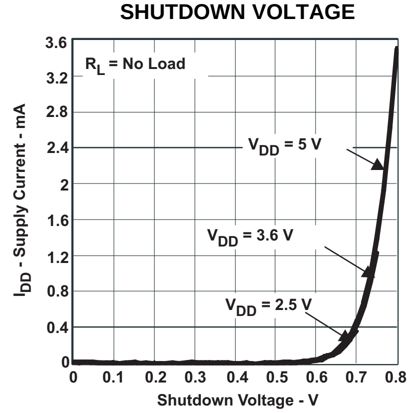


Figure 8.

OUTPUT POWER vs LOAD RESISTANCE

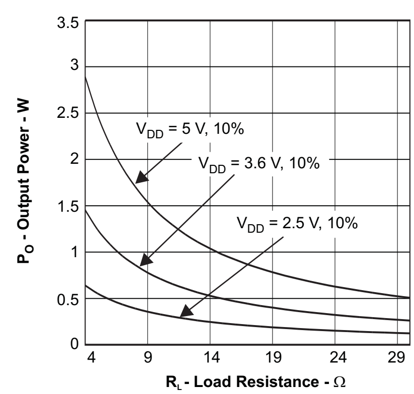


Figure 9.

OUTPUT POWER vs LOAD RESISTANCE

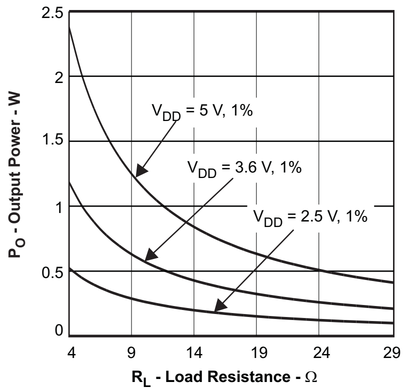


Figure 10.

OUTPUT POWER vs SUPPLY VOLTAGE

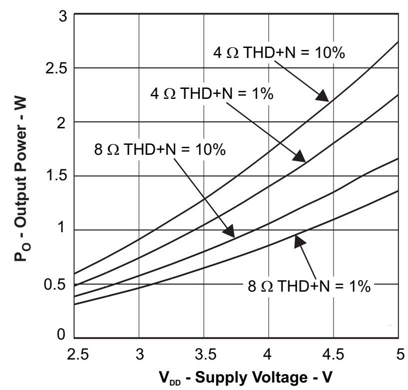


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

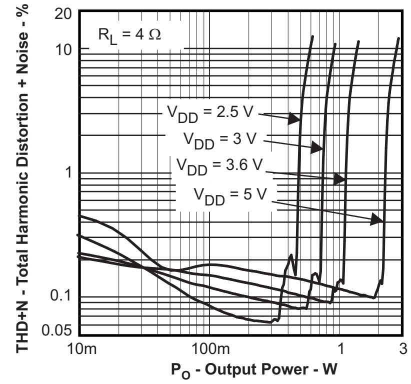


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

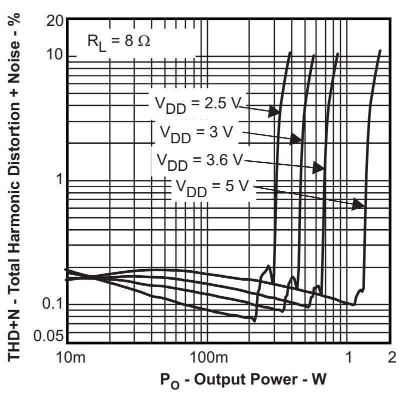


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

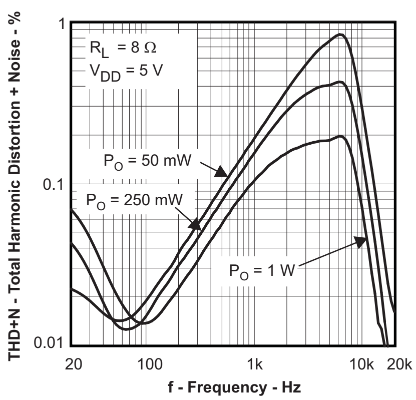


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

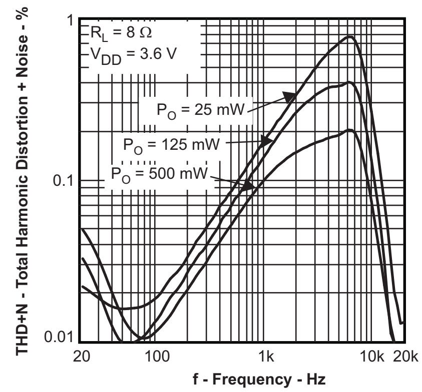


Figure 15.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

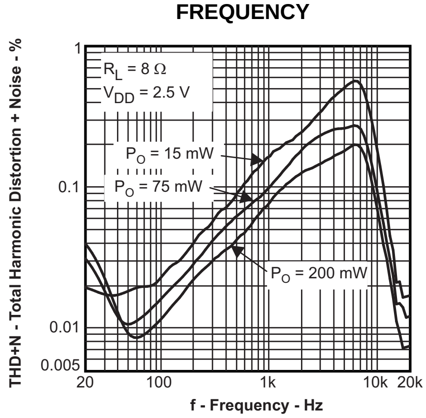


Figure 16.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

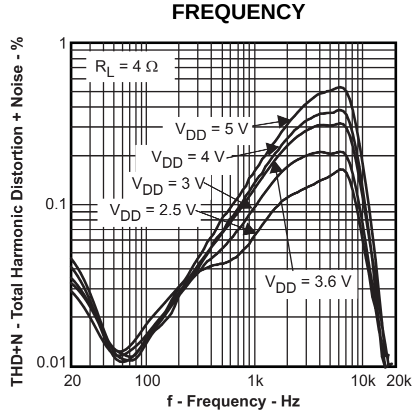


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs COMMON MODE INPUT VOLTAGE

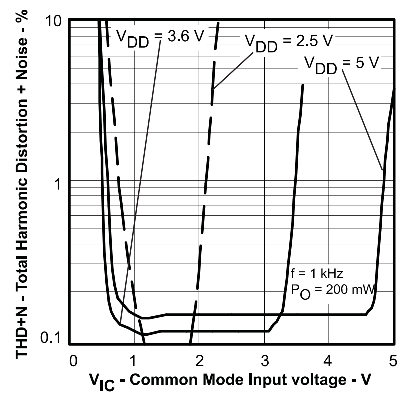


Figure 18.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - TPA2032D1

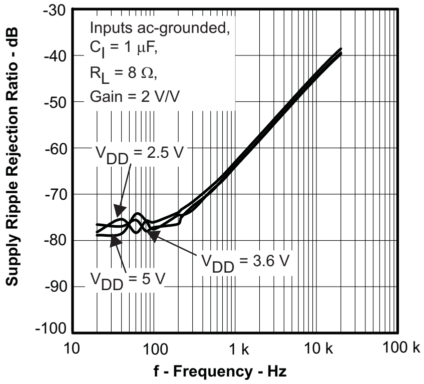


Figure 19.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - TPA2033D1

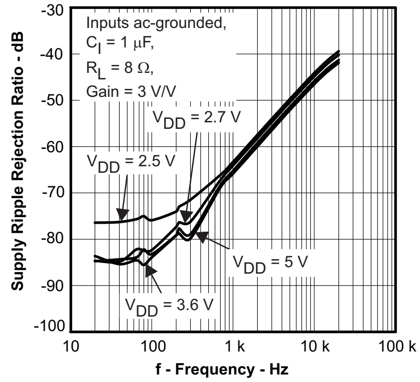


Figure 20.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - TPA2034D1

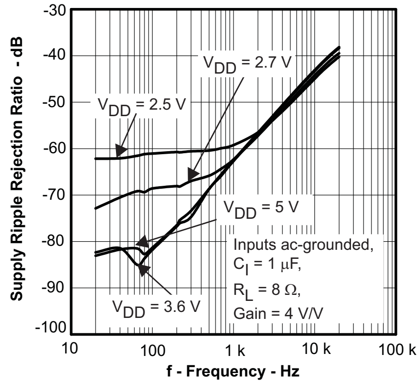


Figure 21.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY- TPA2032D1

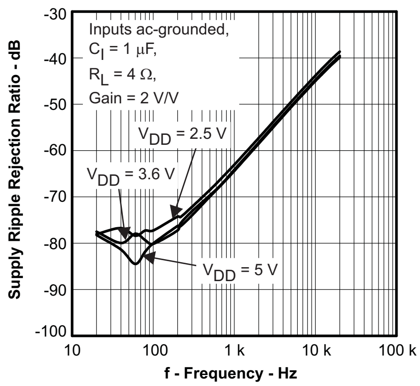


Figure 22.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY- TPA2033D1

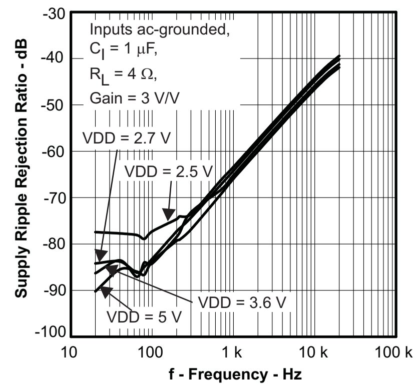


Figure 23.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY- TPA2034D1

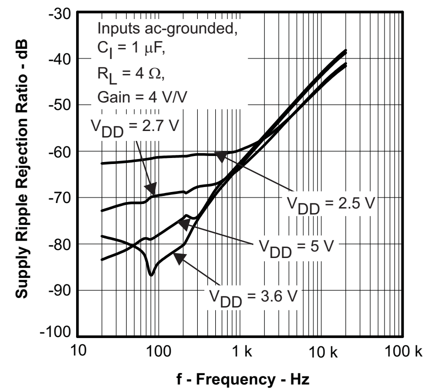


Figure 24.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - TPA2032D1

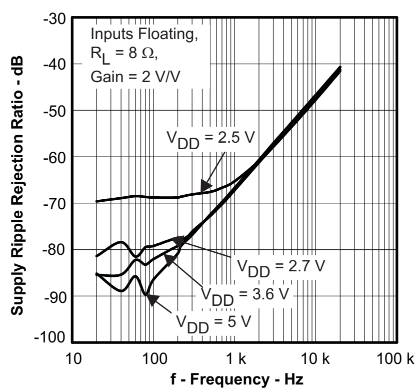


Figure 25.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - TPA2033D1

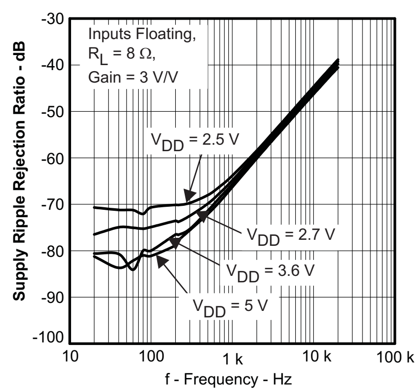


Figure 26.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY - TPA2034D1

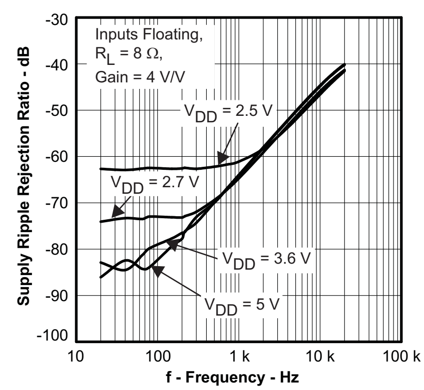


Figure 27.

GSM POWER SUPPLY REJECTION vs TIME

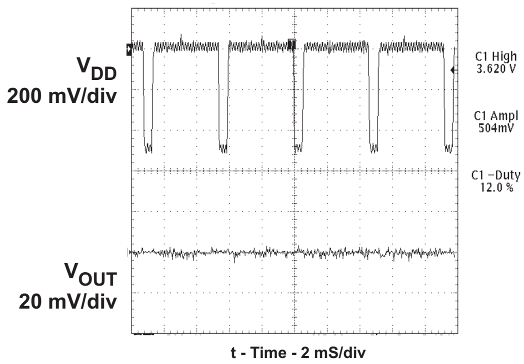


Figure 28.

GSM POWER SUPPLY REJECTION vs FREQUENCY

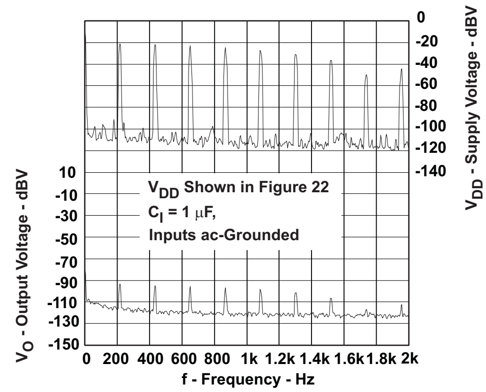


Figure 29.

SUPPLY RIPPLE REJECTION RATIO vs DC COMMON MODE VOLTAGE - TPA2032D1

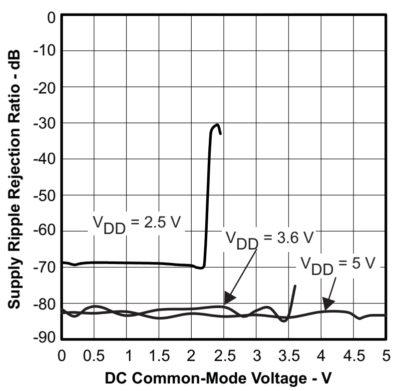


Figure 30.

SUPPLY RIPPLE REJECTION RATIO vs DC COMMON MODE VOLTAGE - TPA2033D1

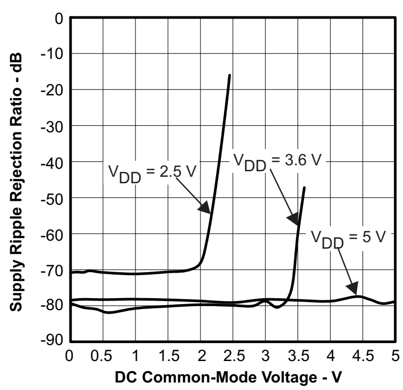


Figure 31.

SUPPLY RIPPLE REJECTION RATIO vs DC COMMON MODE VOLTAGE - TPA2034D1

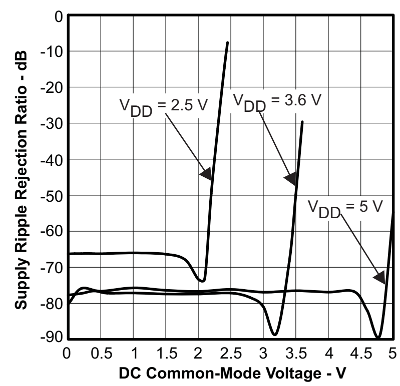


Figure 32.

COMMON-MODE REJECTION RATIO vs FREQUENCY

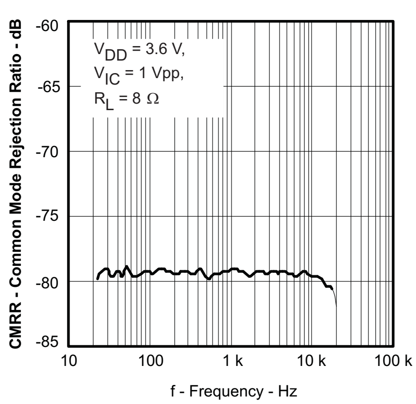


Figure 33.

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

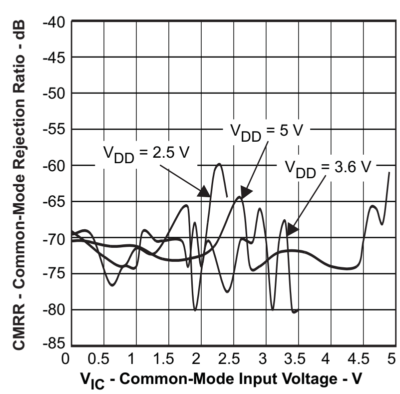


Figure 34.

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA2032D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential TPA2032D1 can still be used with a single-ended input; however, the TPA2032D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
  - The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. The inputs of the TPA2032D1 can be biased anywhere within the common mode input voltage range listed in the Recommended Operating Conditions table. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
  - The fully differential amplifier does not require a bypass capacitor. Any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
  - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal better than the typical audio amplifier.

COMPONENT SELECTION

Figure 35 shows the TPA2032D1 typical schematic with differential inputs, while Figure 36 shows the TPA2032D1 with differential inputs and input capacitors. Figure 37 shows the TPA2032D1 with a single-ended input.

Decoupling Capacitor (C_S)

The TPA2032D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA2032D1 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device. Typically, the smaller the capacitor's case size, the lower the inductance and the closer it can be placed to the TPA2032D1.

Input Capacitors (C_I)

The TPA2032D1 does not require input coupling capacitors if the design uses a differential source that is biased within the common-mode input voltage range. That voltage range is listed in the Recommended Operating Conditions table. If the input signal is not biased within the recommended common-mode input range, such as in needing to use the input as a high pass filter, shown in Figure 36, or if using a single-ended source, shown in Figure 37, input coupling capacitors are required. The same value capacitors should be used on both IN+ and IN– for best pop performance.

$$f_C = \frac{1}{\left(2\pi\, R_I C_I\right)} \tag{1}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speaker response may also be taken into consideration when setting the corner frequency using input capacitors.

APPLICATION INFORMATION (continued)

Equation 2 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{\left(2\pi\, R_I\, f_c\right)} \tag{2}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 µF or larger).

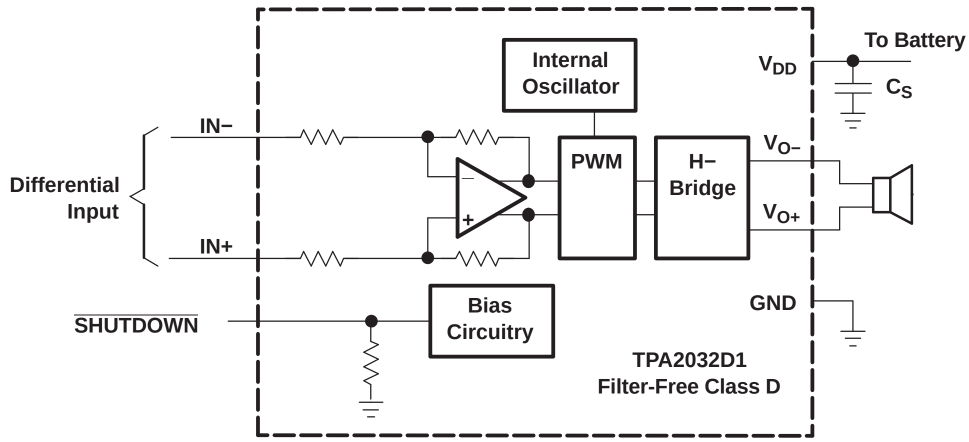


Figure 35. Typical TPA2032D1 Application Schematic With Differential Input for a Wireless Phone

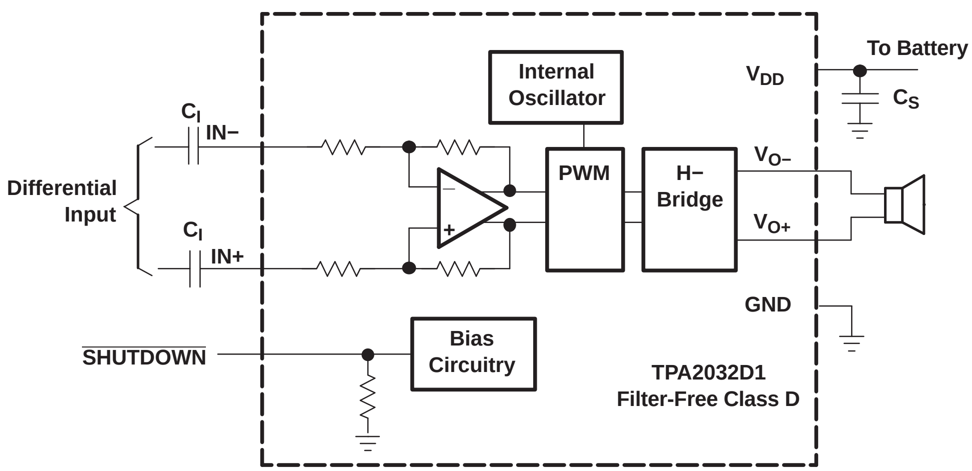


Figure 36. TPA2032D1 Application Schematic With Differential Input and Input Capacitors

APPLICATION INFORMATION (continued)

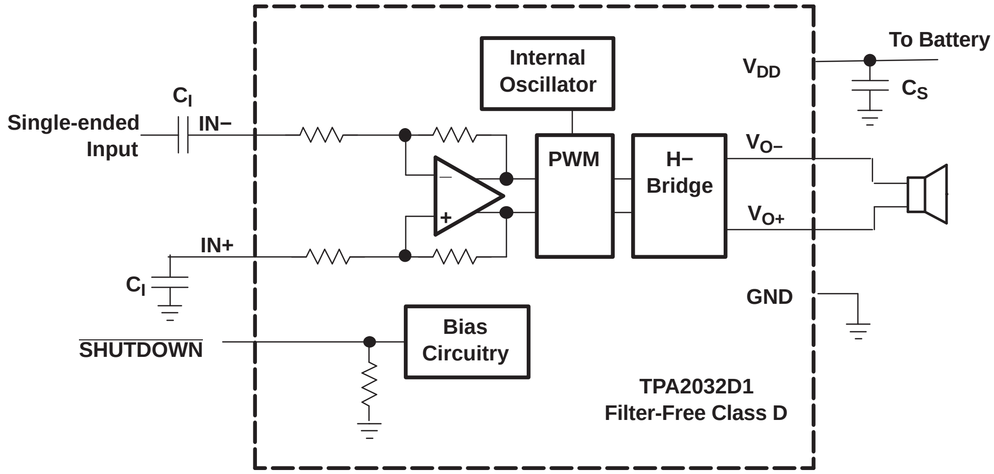


Figure 37. TPA2032D1 Application Schematic With Single-Ended Input

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 38 and Table 1 show the appropriate diameters for a WCSP layout. The TPA2032D1 evaluation module (EVM) layout is shown in the next section as a layout example.

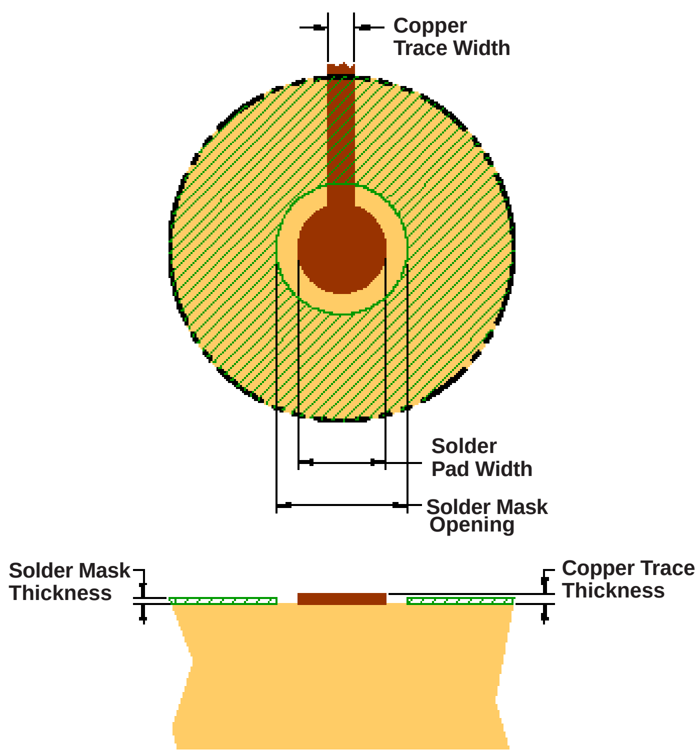


Figure 38. Land Pattern Dimensions

APPLICATION INFORMATION (continued)

Table 1. Land Pattern Dimensions

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 µm (+0.0, –25 µm)	375 µm (+0.0, –25 µm)	1 oz max (32 µm)	275 µm x 275 µm Sq. (rounded corners)	125 µm thick

NOTES:

1. Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
2. Recommended solder paste is Type 3 or Type 4.
3. Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating range of the intended application.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 µm to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
6. Best solder stencil performance is achieved using laser-cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

Component Location

Place all the external components very close to the TPA2032D1. Placing the decoupling capacitor, C_S, close to the TPA2032D1 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Trace Width

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. Figure 39 shows the layout of the TPA2032D1 evaluation module (EVM).

For high current pins (V_{DD}, GND V_{O+}, and V_{O-}) of the TPA2032D1, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device.

For input pins (IN–, IN+, and $\overline{\text{SHUTDOWN}}$) of the TPA2032D1, use 75-µm to 100-µm trace widths at the solder balls. IN– and IN+ traces need to run side-by-side to maximize common-mode noise cancellation.

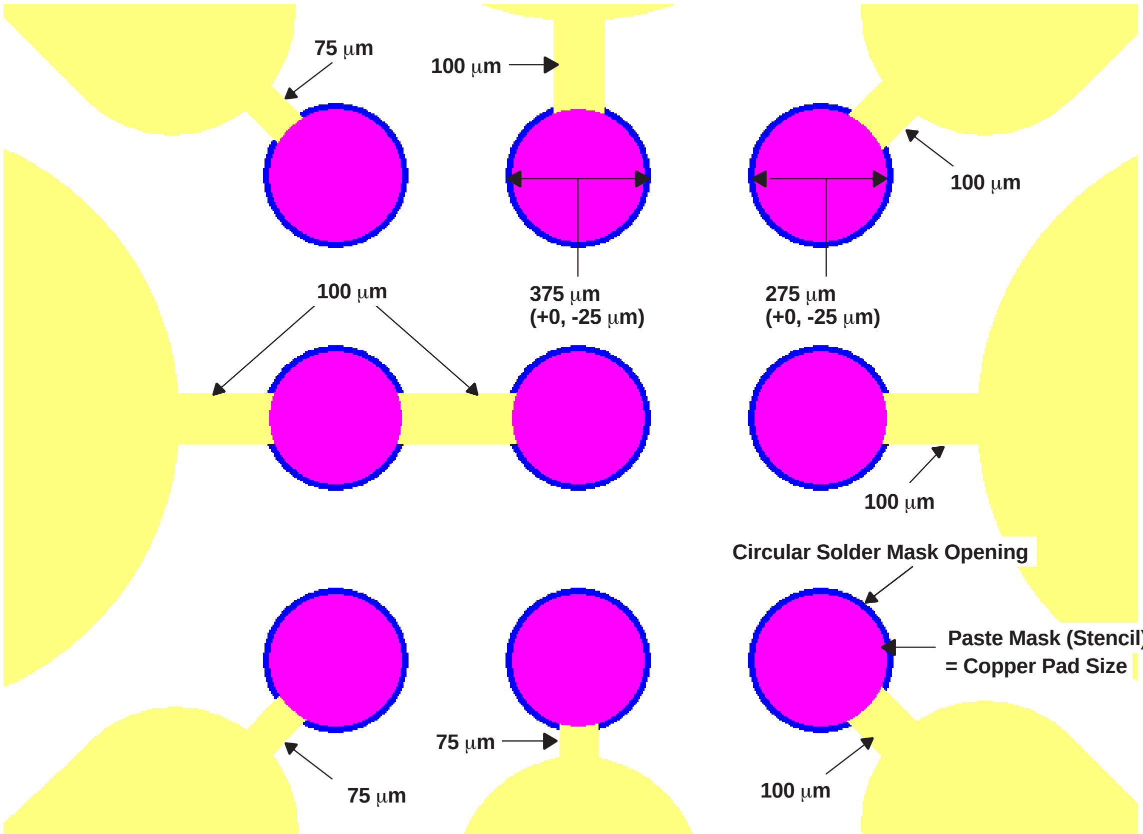


Figure 39. Close Up of TPA2032D1 Land Pattern From TPA2032D1 EVM

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the YZF package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} \quad (3)$$

Given θ_{JA} (from the Package Dissipation ratings table), the maximum allowable junction temperature (from the Absolute Maximum ratings table), and the maximum internal dissipation (from Power Dissipation vs Output Power figures) the maximum ambient temperature can be calculated with the following equation. Note that the units on these figures are Watts RMS. Because of crest factor (ratio of peak power to RMS power) from 9–15 dB, thermal limitations are not usually encountered.

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{Dmax} \quad (4)$$

The TPA2032D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Note that using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier. θ_{JA} is a gross approximation of the complex thermal transfer mechanisms between the device and its ambient environment. If the θ_{JA} calculation reveals a potential problem, a more accurate estimate should be made. Please contact TI for further information.

WHEN TO USE AN OUTPUT FILTER

Design the TPA2032D1 without an output filter if the traces from the amplifier to the speaker are short. Wireless handsets and PDAs are great applications for this class-D amplifier to be used without an output filter.

The TPA2032D1 passed FCC- and CE-radiated emissions testing with no shielding with speaker trace wires 100 mm long or less. For longer speaker trace wires, a ferrite bead can often be used in the design if failing radiated emissions testing without an LC filter; and, the frequency-sensitive circuit is greater than 1 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. The selection must also take into account the currents flowing through the ferrite bead. Ferrites can begin to loose effectiveness at much lower than rated current values. Please see the EVM User's Guide for components used successfully by TI.

Figure 40 shows a typical ferrite-bead output filter.

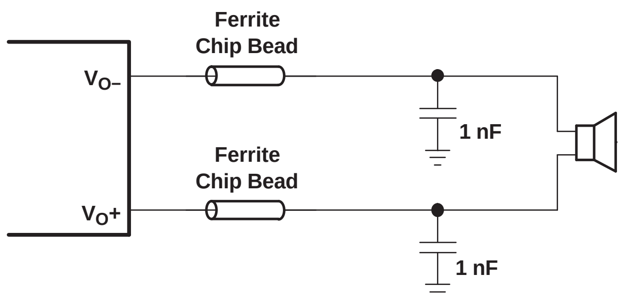
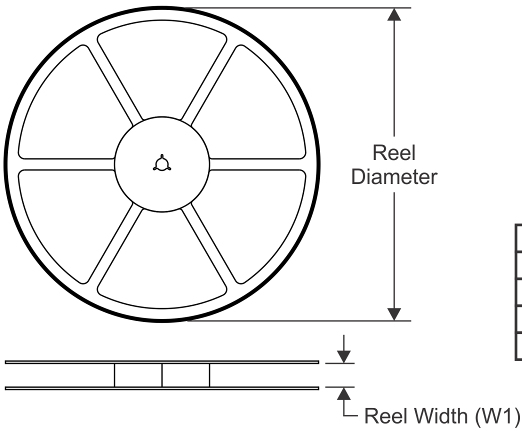


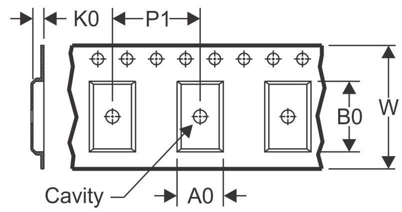
Figure 40. Typical Ferrite Chip Bead Filter

TAPE AND REEL INFORMATION

REEL DIMENSIONS

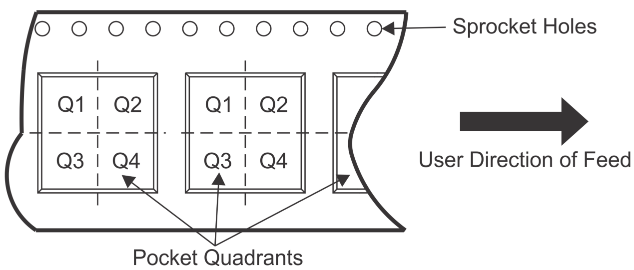


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

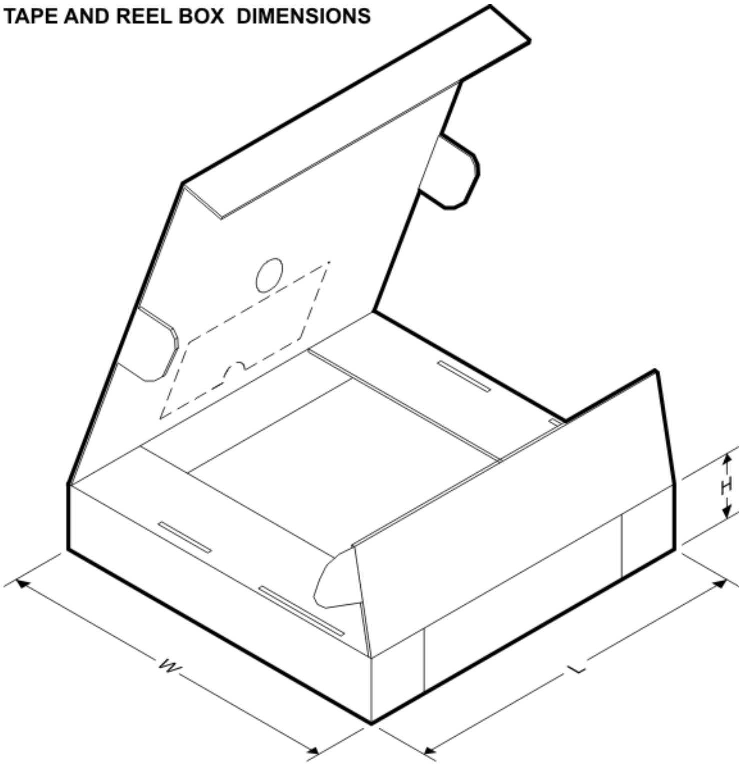
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2033D1YZFR	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPA2033D1YZFT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPA2034D1YZFR	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPA2034D1YZFT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

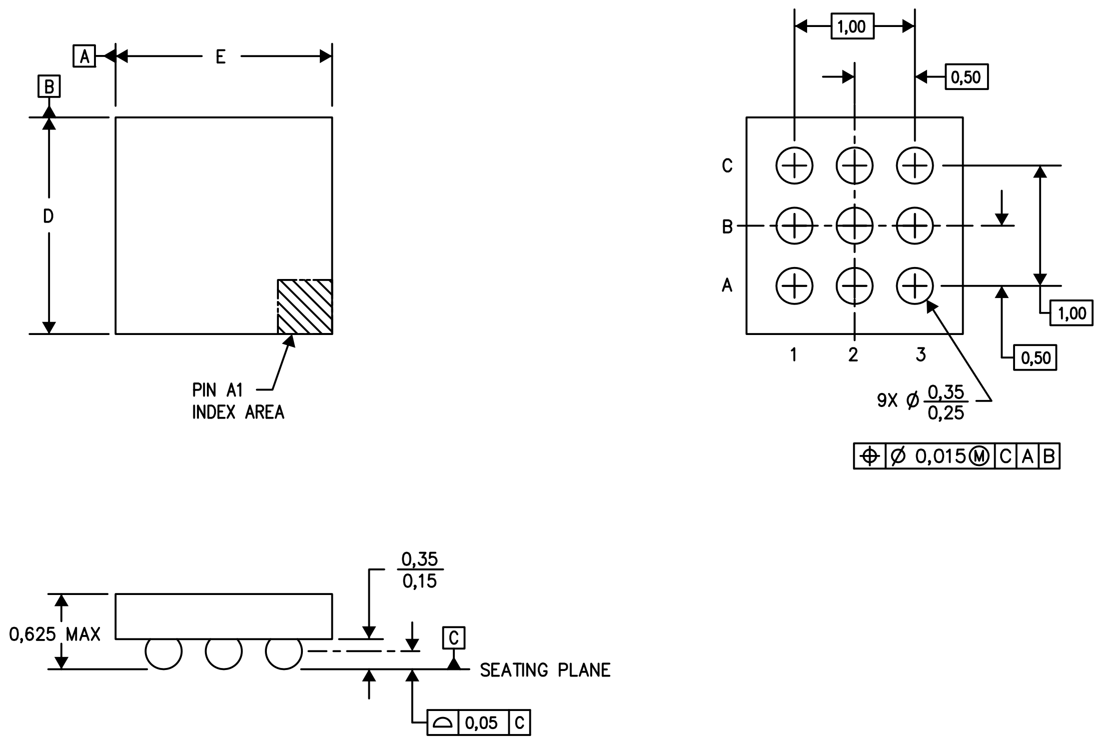
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2033D1YZFR	DSBGA	YZF	9	3000	210.0	185.0	35.0
TPA2033D1YZFT	DSBGA	YZF	9	250	210.0	185.0	35.0
TPA2034D1YZFR	DSBGA	YZF	9	3000	210.0	185.0	35.0
TPA2034D1YZFT	DSBGA	YZF	9	250	210.0	185.0	35.0

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



4205058–4/P 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265