

# TLC540I, TLC541I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

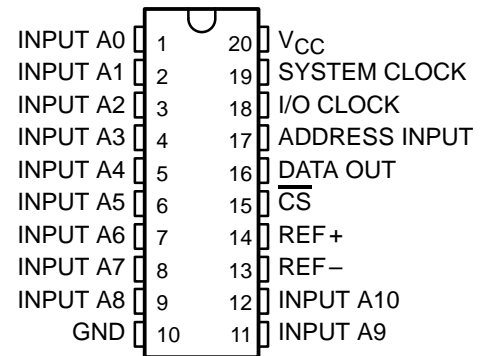
- 8-Bit Resolution A/D Converter
- Microprocessor Peripheral or Stand-Alone Operation
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . .  $\pm 0.5$  LSB Max
- TLC541 Is Direct Replacement for Motorola MC145040 and National Semiconductor ADC0811. TLC540 Is Capable of Higher Speed
- Pinout and Control Signals Compatible With TLC1540 Family of 10-Bit A/D Converters
- CMOS Technology

PARAMETER	TLC540	TLC541
Channel Acquisition Sample Time	2 $\mu$ s	3.6 $\mu$ s
Conversion Time (Max)	9 $\mu$ s	17 $\mu$ s
Samples per Second (Max)	75 x 10 <sup>3</sup>	40 x 10 <sup>3</sup>
Power Dissipation (Max)	12.5 mW	12.5 mW

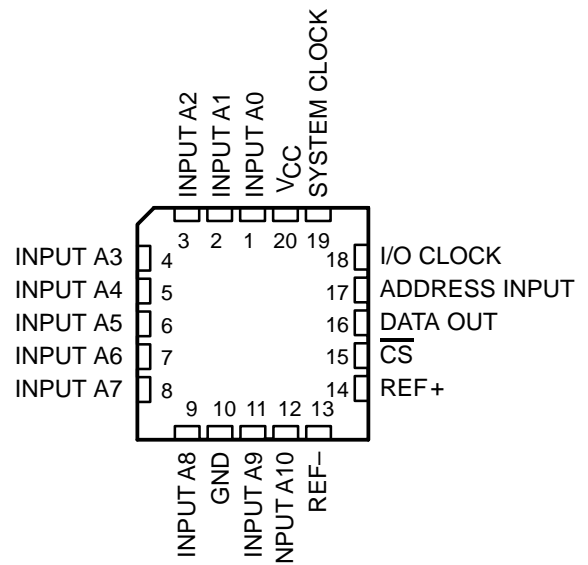
## description

The TLC540 and TLC541 are CMOS A/D converters built around an 8-bit switched-capacitor successive-approximation A/D converters. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs, including independent SYSTEM CLOCK, I/O CLOCK, chip select (CS), and ADDRESS INPUT. A 4-MHz system clock for the TLC540 and a 2.1-MHz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

DW OR N PACKAGE  
(TOP VIEW)



FN PACKAGE  
(TOP VIEW)



## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE		
	SO PLASTIC DIP (DW)	PLASTIC DIP (N)	CHIP CARRIER (FN)
-40°C to 85°C	— TLC541IDW	TLC540IN TLC541IN	TLC540IFN TLC541IFN
-55°C to 125°C	—	TLC541MN	—



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

# TLC540I, TLC541I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 INPUTS

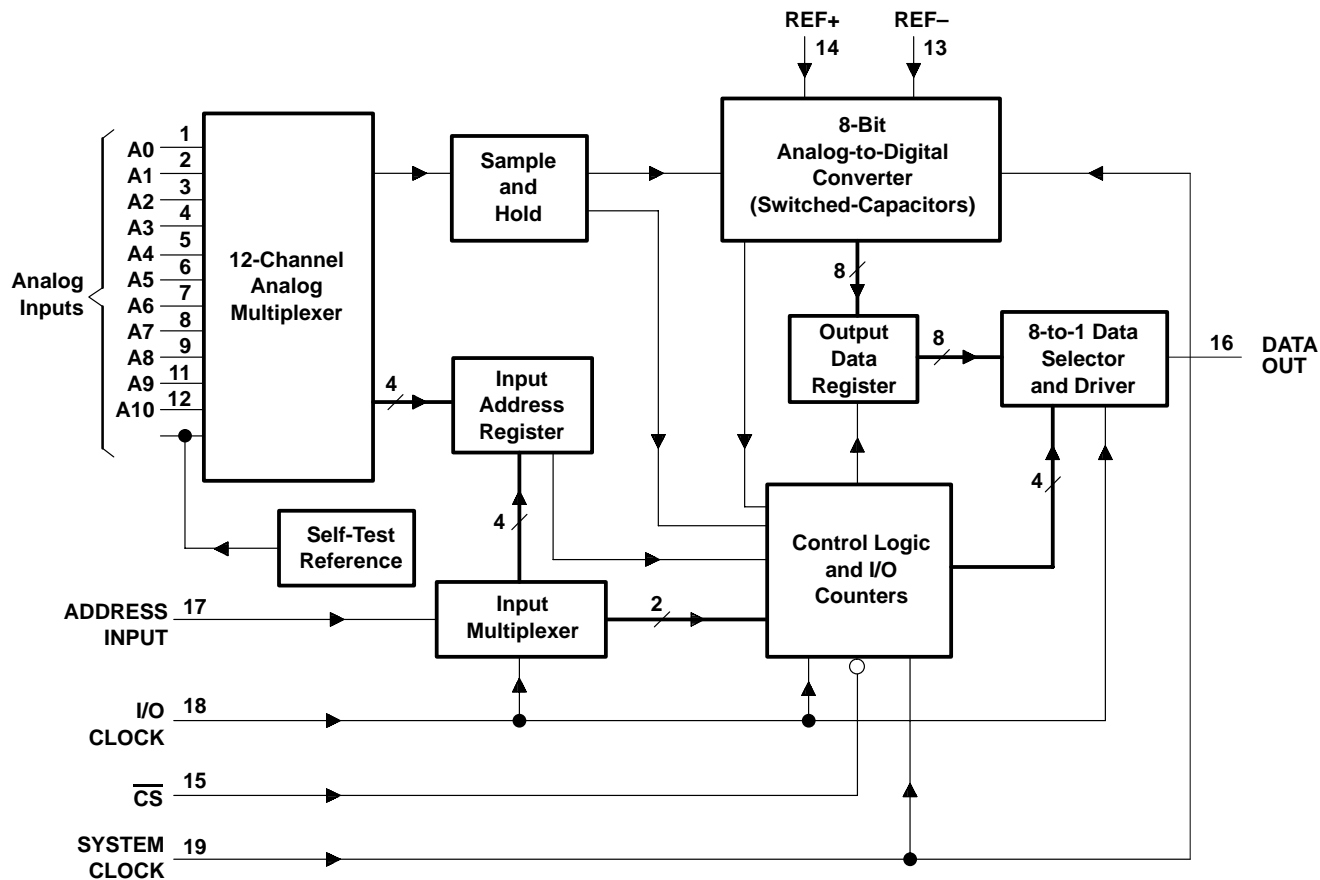
SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

## description (continued)

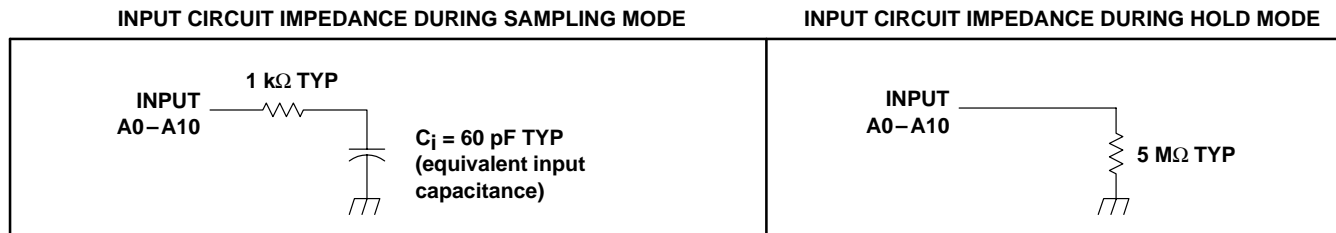
The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows low-error ( $\pm 0.5$  LSB) conversion in  $9 \mu\text{s}$  for the TLC540 and  $17 \mu\text{s}$  for the TLC541 over the full operating temperature range.

The TLC540I and TLC541I are characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The TLC541M is characterized for operation from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

## functional block diagram



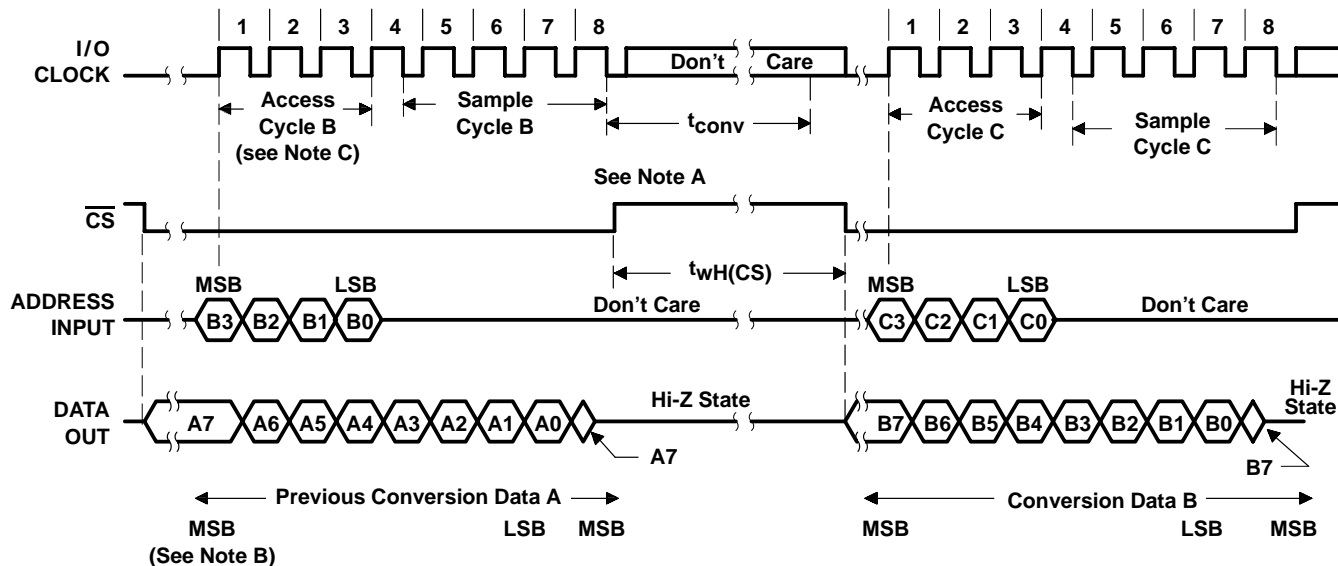
## typical equivalent inputs



**TLC5401, TLC5411**  
**8-BIT ANALOG-TO-DIGITAL CONVERTERS**  
**WITH SERIAL CONTROL AND 11 INPUTS**

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

**operating sequence**



- NOTES:
- A. The conversion cycle, which requires 36 system clock periods, is initiated on the 8th falling edge of I/O CLOCK after  $\overline{CS}$  goes low for the channel whose address exists in memory at that time. If  $\overline{CS}$  is kept low during conversion, I/O CLOCK must remain low for at least 36 system clock cycles to allow conversion to be completed.
  - B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after  $\overline{CS}$  is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.
  - C. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	6.5 V
Input voltage range, $V_I$ (any input)	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, $V_O$	–0.3 V to $V_{CC} + 0.3$ V
Peak input current range (any input)	±10 mA
Peak total input current (all inputs)	±30 mA
Operating free-air temperature range, $T_A$ : TLC5401, TLC5411	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF– and GND wired together (unless otherwise noted).



# TLC540I, TLC541I

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL AND 11 INPUTS

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

#### recommended operating conditions

	TLC540			TLC541			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, $V_{CC}$	4.75	5	5.5	4.75	5	5.5	V	
Positive reference voltage, $V_{ref+}$ (see Note 2)	2.5	$V_{CC}$	$V_{CC}+0.1$	2.5	$V_{CC}$	$V_{CC}+0.1$	V	
Negative reference voltage, $V_{ref-}$ (see Note 2)	-0.1	0	2.5	-0.1	0	2.5	V	
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)	1	$V_{CC}$	$V_{CC}+0.2$	1	$V_{CC}$	$V_{CC}+0.2$	V	
Analog input voltage (see Note 2)	0		$V_{CC}$	0		$V_{CC}$	V	
High-level control input voltage, $V_{IH}$	2			2			V	
Low-level control input voltage, $V_{IL}$			0.8			0.8	V	
Setup time, address bits at data input before I/O CLOCK $\uparrow$ , $t_{su}(A)$	200			400			ns	
Hold time, address bits after I/O CLOCK $\uparrow$ , $t_h(A)$	0			0			ns	
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su}(CS)$ (see Note 3)	3			3			System clock cycles	
$\overline{CS}$ high during conversion, $t_{WH}(CS)$	36			36			System clock cycles	
I/O CLOCK frequency, $f_{clock(I/O)}$	0		2.048	0		1.1	MHz	
Pulse duration, SYSTEM CLOCK frequency, $f_{clock(SYS)}$	$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz	
Pulse duration, SYSTEM CLOCK high, $t_{WH}(SYS)$	110			210			MHz	
Pulse duration, SYSTEM CLOCK low, $t_{WL}(SYS)$	100			190			MHz	
Pulse duration, I/O clock high, $t_{WH}(I/O)$	200			404			ns	
Pulse duration, I/O clock low, $t_{WL}(I/O)$	200			404			ns	
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \leq 1048$ kHz	30		30		ns	
		$f_{clock(SYS)} > 1048$ kHz	20		20			
	I/O	$f_{clock(I/O)} \leq 525$ kHz	100		100			
		$f_{clock(I/O)} > 525$ kHz	40		40			
Operating free-air temperature, $T_A$	TLC540I, TLC541I		-40	85		-40	85	°C

- NOTES: 2. Analog input voltages greater than that applied to REF + convert as all 1s (11111111), while input voltages less than that applied to REF- convert as all 0s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
3. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for three SYSTEM CLOCK cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip select setup time has elapsed.
4. This is the time required for the clock input signal to fall from  $V_{IH}$  min to  $V_{IL}$  max or to rise from  $V_{IL}$  max to  $V_{IH}$  min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2  $\mu$ s for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



**TLC540I, TLC541I**  
**8-BIT ANALOG-TO-DIGITAL CONVERTERS**  
**WITH SERIAL CONTROL AND 11 INPUTS**

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

electrical characteristics over recommended operating temperature range,  $V_{CC} = V_{ref+} = 4.75\text{ V}$  to  $5.5\text{ V}$ ,  $f_{clock(I/O)} = 2.048\text{ MHz}$  for TLC540 or  $f_{clock(I/O)} = 1.1\text{ MHz}$  for TLC541 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$	High-level output voltage, DATA OUT	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = 360\text{ }\mu\text{A}$	2.4			V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 1.6\text{ mA}$			0.4	V
$I_{OZ}$	Off-state (high-impedance state) output current	$V_O = V_{CC}$ , $\overline{CS}$ at $V_{CC}$			10	$\mu\text{A}$
		$V_O = 0$ , $\overline{CS}$ at $V_{CC}$			-10	
$I_{IH}$	High-level input current	$V_I = V_{CC}$		0.005	2.5	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0$		-0.005	-2.5	$\mu\text{A}$
$I_{CC}$	Operating supply current	$\overline{CS}$ at 0 V		1.2	2.5	mA
Selected channel leakage current		Selected channel at $V_{CC}$ , Unselected channel at 0 V		0.4	1	$\mu\text{A}$
		Selected channel at 0 V, Unselected channel at $V_{CC}$		-0.4	-1	
$I_{CC} + I_{ref}$	Supply and reference current	$V_{ref+} = V_{CC}$ , $\overline{CS}$ at 0 V		1.3	3	mA
$C_i$	Input capacitance	Analog inputs		7	55	$\text{pF}$
		Control inputs		5	15	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

# TLC540I, TLC541I

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL AND 11 INPUTS

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

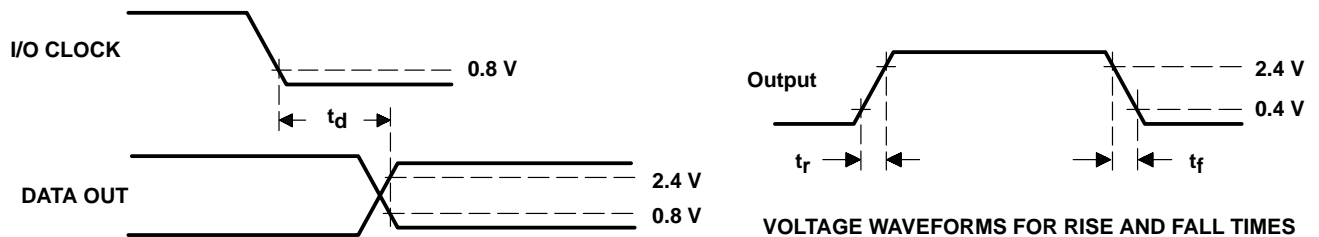
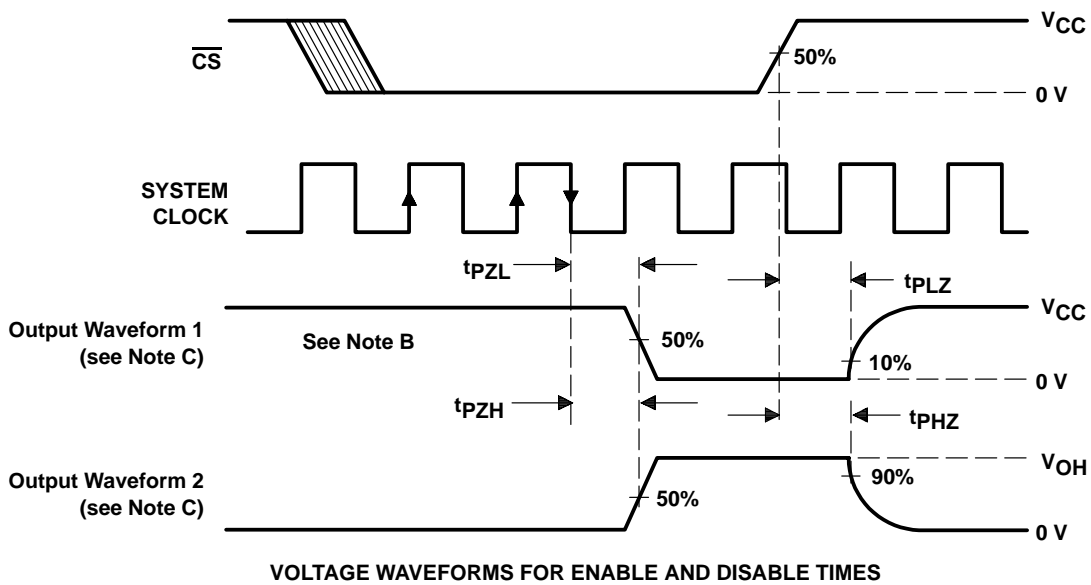
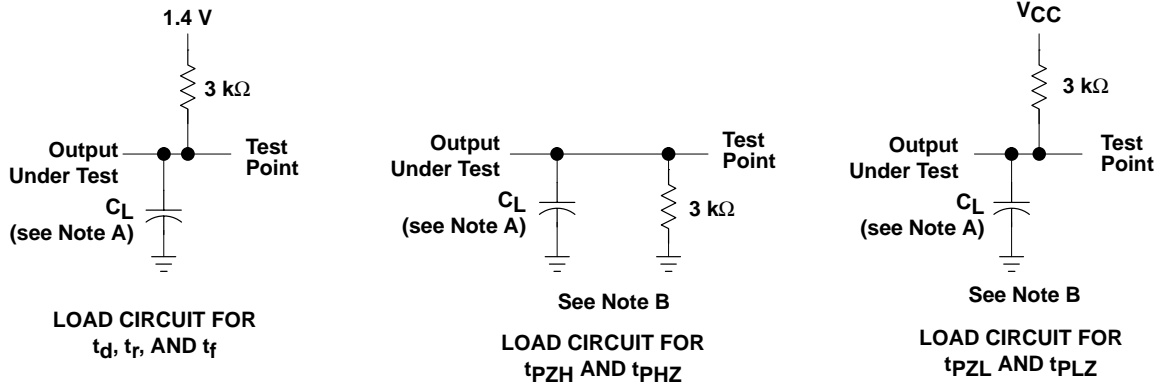
operating characteristics over recommended operating free-air temperature range,  
 $V_{CC} = V_{ref+} - 4.75\text{ V to } 5.5\text{ V}$ ,  $f_{clock(I/O)} = 2.048\text{ MHz for TLC540 or } 1.1\text{ MHz for TLC541}$ ,  
 $f_{clock(SYS)} = 4\text{ MHz for TLC540 or } 2.1\text{ MHz for TLC541}$

PARAMETER	TEST CONDITIONS	TLC540		TLC541		UNIT
		MIN	MAX	MIN	MAX	
$E_L$ Linearity error	See Note 5	±0.5		±0.5		LSB
$E_{ZS}$ Zero-scale error	See Notes 2 and 6	±0.5		±0.5		LSB
$E_{FS}$ Full-scale error	See Notes 2 and 6	±0.5		±0.5		LSB
Total unadjusted error	See Note 7	±0.5		±0.5		LSB
Self-test output code	Input A11 address = 1011, (see Note 8)	01111101 (125)	10000011 (131)	01111101 (125)	10000011 (131)	
$t_{conv}$ Conversion time	See operating sequence	9		17		μs
Total access and conversion time	See operating sequence	13.3		25		μs
$t_a$ Channel acquisition time (sample cycle)	See operating sequence	4		4		I/O clock cycles
$t_v$ Time output data remains valid after I/O CLOCK↓		10		10		ns
$t_d$ Delay time, I/O CLOCK↓ to data output valid	See Parameter Measurement Information	300		400		ns
$t_{en}$ Output enable time		150		150		ns
$t_{dis}$ Output disable time		150		150		ns
$t_{r(bus)}$ Data bus rise time		300		300		ns
$t_{f(bus)}$ Data bus fall time		300		300		ns

- NOTES:
- Analog input voltages greater than that applied to REF+ convert to all 1s (11111111) while input voltages less than that applied to REF- convert to all 0s (00000000). For proper operation, REF+ voltage must be at least 1 V higher than REF- voltage. Also, the total unadjusted error may increase as this differential reference voltage falls below 4.75 V.
  - Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
  - Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
  - Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
  - Both the input address and the output codes are expressed in positive logic.



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L = 50$  pF for TLC540 and 100 pF for TLC541.  
 B.  $t_{en} = t_{pZH}$  or  $t_{pZL}$ ,  $t_{dis} = t_{pHZ}$  or  $t_{pLZ}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

**TLC540I, TLC541I**  
**8-BIT ANALOG-TO-DIGITAL CONVERTERS**  
**WITH SERIAL CONTROL AND 11 INPUTS**

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

**APPLICATION INFORMATION**

**simplified analog input analysis**

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to  $V_S$  within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left( 1 - e^{-t_c / R_t C_i} \right) \tag{1}$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/512) \tag{2}$$

Equating equation 1 to equation 2 and solving for time  $t_c$  gives

$$V_S - (V_S/512) = V_S \left( 1 - e^{-t_c / R_t C_i} \right) \tag{3}$$

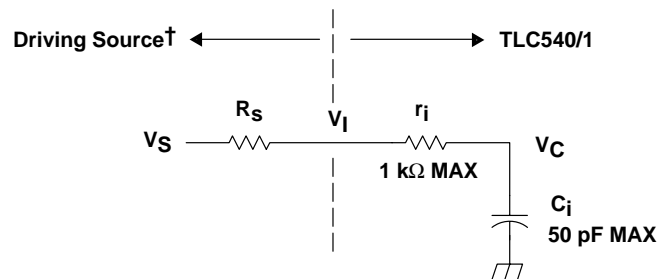
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(512) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



$V_I$  = Input Voltage at INPUT A0–A10  
 $V_S$  = External Driving Source Voltage  
 $R_S$  = Source Resistance  
 $r_i$  = Input Resistance  
 $C_i$  = Equivalent Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- $R_S$  must be real at the input frequency.

**Figure 1. Equivalent Input Circuit Including the Driving Source**



---

## PRINCIPLES OF OPERATION

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ( $\overline{CS}$ ), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 9  $\mu$ s, while complete input-conversion-output cycles can be repeated every 13  $\mu$ s. With TLC541 a conversion can be completed in 17  $\mu$ s, while complete input-conversion-output cycles are repeated every 25  $\mu$ s. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in self-test and in any order desired by the controlling processor.

The system and I/O clocks are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to SYSTEM CLOCK, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using I/O CLOCK. SYSTEM CLOCK will drive the conversion crunching circuitry so that the control hardware and software need not be concerned with this task.

When  $\overline{CS}$  is high, DATA OUT is in a 3-state condition and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of  $\overline{CS}$ , to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC540/541 devices are used. In this way, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1.  $\overline{CS}$  is brought low. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for two rising edges and then a falling edge of SYSTEM CLOCK after a low  $\overline{CS}$  transition, before the low transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first four rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these four I/O clock pulses shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fourth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to I/O CLOCK and the sixth, seventh, and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle,  $\overline{CS}$  must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$  can be kept low during periods of multiple conversion. When keeping  $\overline{CS}$  low during periods of multiple conversion, special care must be exercised to prevent noise glitches on I/O CLOCK. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if  $\overline{CS}$  is taken high, it must remain high until the end of the conversion. Otherwise, a valid falling edge of  $\overline{CS}$  causes a reset condition, which aborts the conversion in progress.

A new conversion can be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

# TLC540I, TLC541I

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL AND 11 INPUTS

SLAS065B – OCTOBER 1983 – REVISED JUNE 2001

---

#### PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O clock together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. The first two clocks are required for this device to recognize  $\overline{CS}$  is at a valid low level when the common clock signal is used as an I/O CLOCK. When  $\overline{CS}$  is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low  $\overline{CS}$  must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a  $\overline{CS}$  transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a  $\overline{CS}$  negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address,  $\overline{CS}$  must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and will shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle until the moment at which the analog signal must be converted. The TLC540/TLC541 continues sampling the analog input until the eighth falling edge of the I/O clock. The control circuitry or software then immediately lowers the I/O clock signal and holds the analog signal at the desired point in time and start conversion.

Detailed information on interfacing to most popular microprocessors is readily available from the factory.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLC540IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC540IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC540IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC540IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC540IFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC540IFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC540IFNR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC540IFNRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC540IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC540INE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC541IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC541IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC541IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC541IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC541IFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC541IFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC541IFNR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC541IFNRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC541IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC541INE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC541INS	ACTIVE	SO	NS	20	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC541INSG4	ACTIVE	SO	NS	20	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC541MN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

---

a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

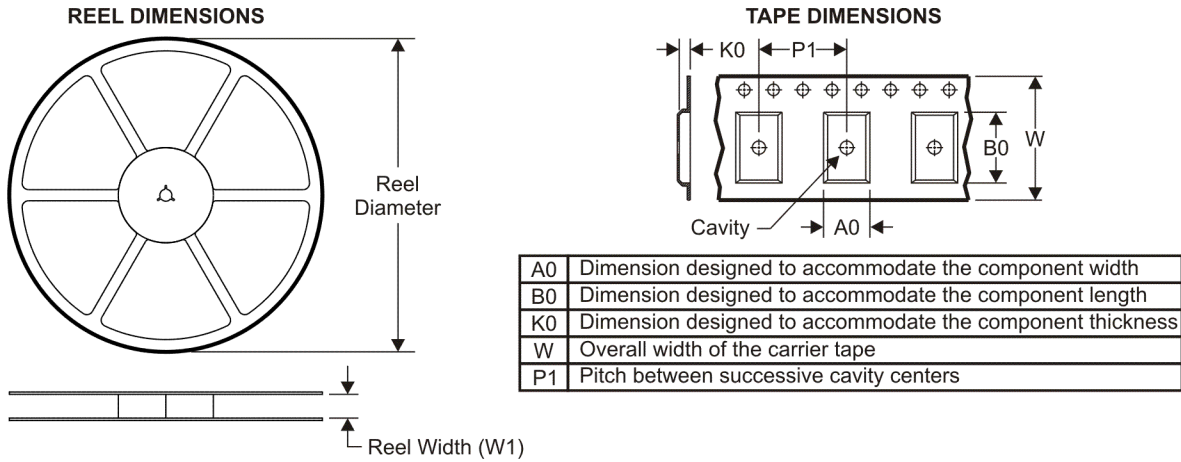
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

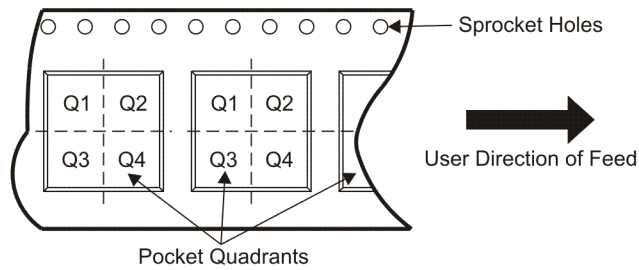
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**



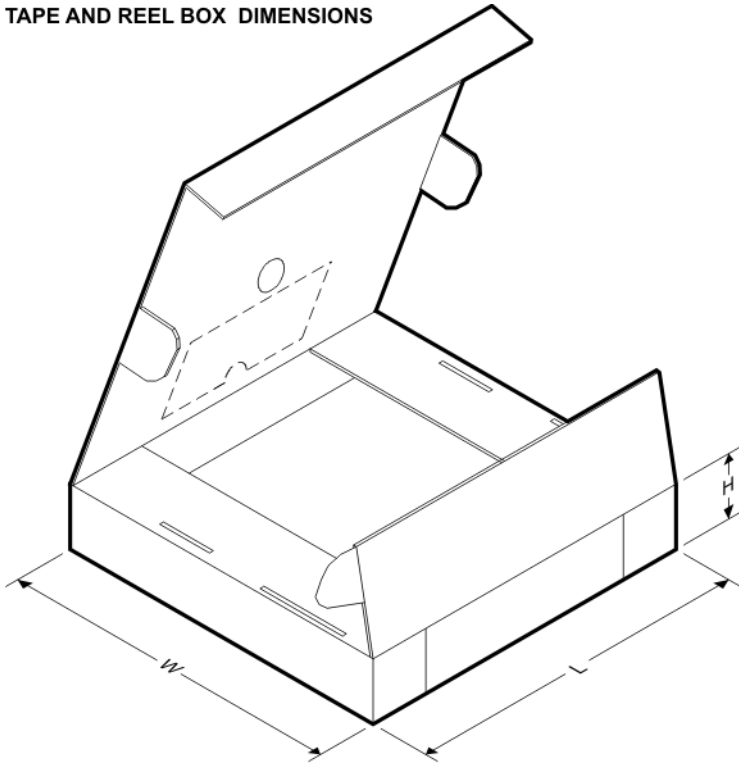
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC540IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1
TLC541IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC540IDWR	SOIC	DW	20	2000	346.0	346.0	41.0
TLC541IDWR	SOIC	DW	20	2000	346.0	346.0	41.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

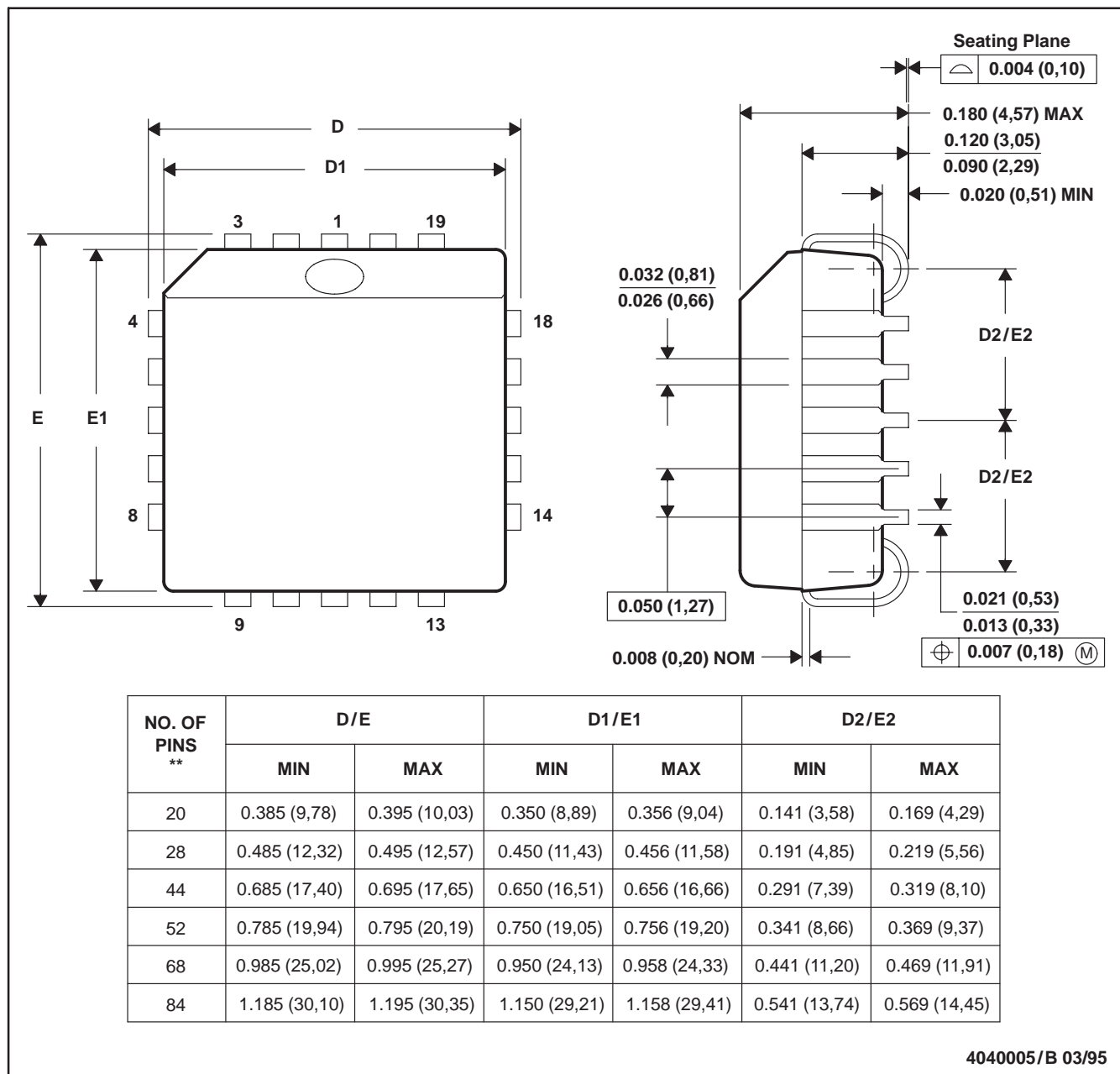


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

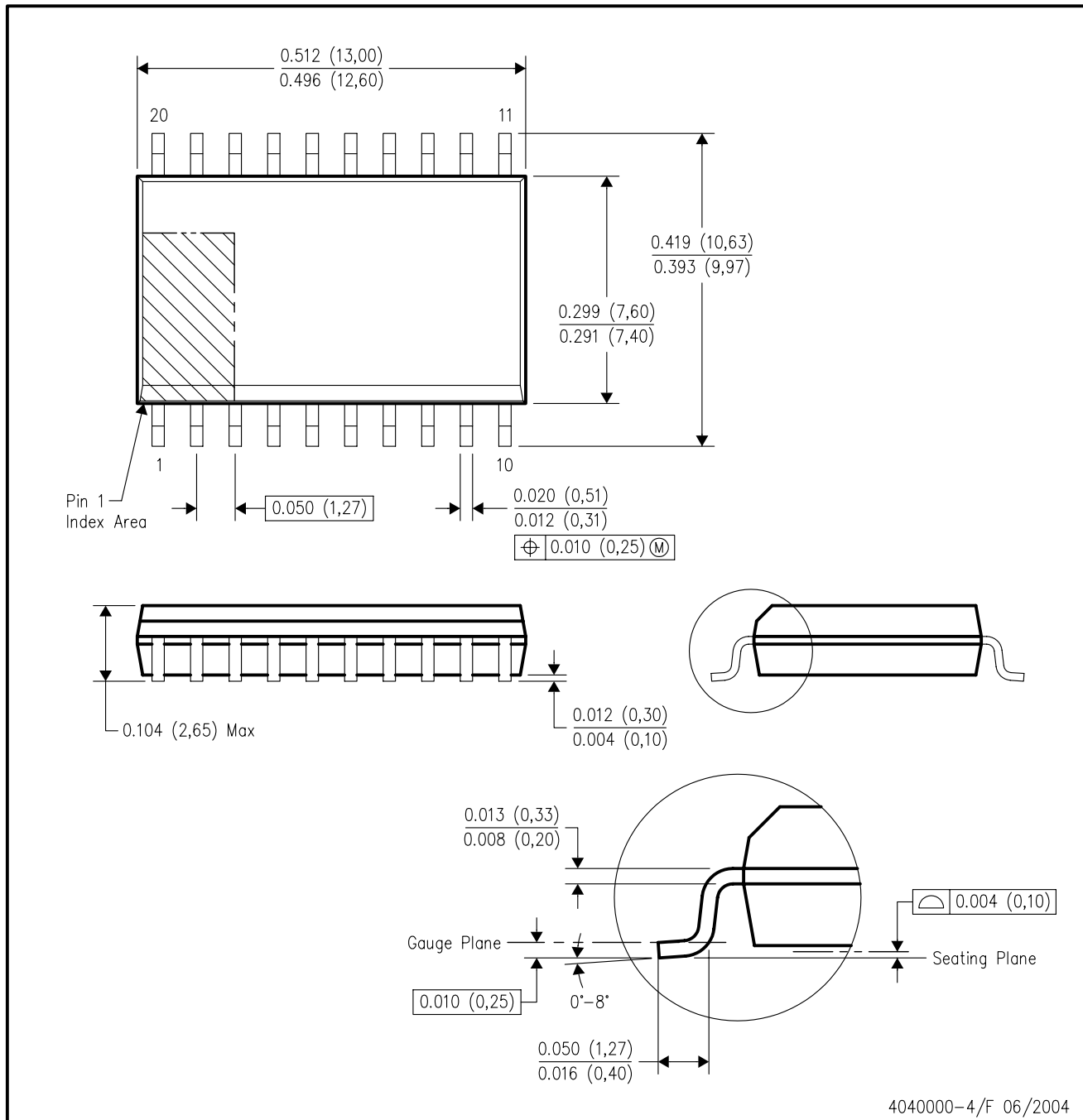


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated