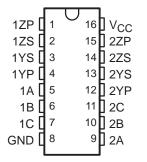
- Choice of Open-Collector, Open-Emitter, or Totem-Pole Outputs
- Single-Ended or Differential AND/NAND Outputs
- Single 5-V Supply
- Dual-Channel Operation
- TTL Compatible
- Short-Circuit Protection
- High-Current Outputs
- Triple inputs
- Clamp Diodes at Inputs and Outputs
- Designed for Use With SN55115 and SN75115 Differential Line Receivers
- Designed to Be Interchangeable With National DS9614 Line Driver

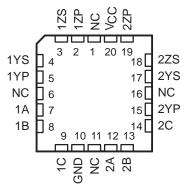
description

The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with the high-current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL-compatible output levels, these devices can also be used as TTL expanders or phase splitters.

SN55114...J OR W PACKAGE SN75114...D OR N PACKAGE (TOP VIEW)



SN55114 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN55114 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN75114 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

	INPUTS	OUTI	PUTS	
Α	В	С	Υ	Z
Н	Н	Н	Н	L
All other	input comb	L	Н	

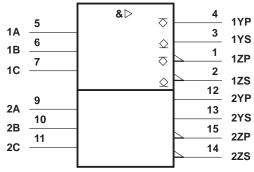
H = high level, L = low level



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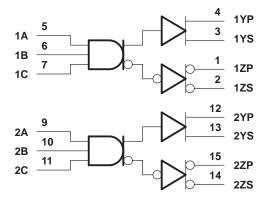
logic symbol†



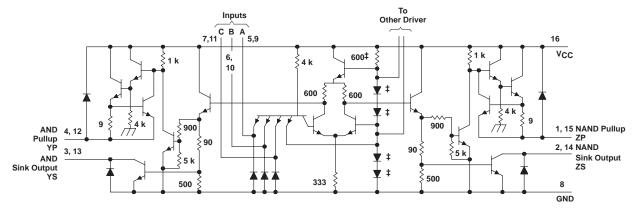
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic (each driver)



[‡]These components are common to both drivers. Resistor values shown are nominal and in ohms. Pin numbers shown are for the D, J, N, and W packages.



SLLS071C - SEPTEMBER 1973 - REVISED SEPTEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage, V _I	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T _{Stg}	
Case temperature for 60 seconds, T _c : FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	,
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package	ne 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	_
FK [‡]	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	_
w‡	1000 mW	8.0 mW/°C	640 mW	200 mW

[‡] In the FK, J, and W packages, SN55114 chips are either silver glass or alloy mounted.

recommended operating conditions (unless otherwise noted)

	9	SN55114		9	N75114		UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, VIH	2			2			V
Low-level input voltage, V _{IL}			0.8			0.8	V
High-level output current, IOH			-40			-40	mA
Low-level output current, IOL			40			40	mA
Operating free-air temperature, T _A	-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS [†]			,	SN55114	l	SN75114			UNIT	
	PARAMETER	Т	TEST CONDITIONS				MAX	MIN	TYP‡	MAX	0.411	
VIK	Input clamp voltage	$V_{CC} = MIN,$	$I_{I} = -12 \text{ mA}$			-0.9	-1.5		-0.9	-1.5	V	
VOH	High-level output	V _{CC} = MIN,	V _{IH} = 2 V,	$I_{OH} = -10 \text{ mA}$	2.4	3.4		2.4	3.4		V	
VOH	voltage	V _{IL} = 0.8 V		$I_{OH} = -40 \text{ mA}$	2	3		2	3		V	
V _{OL}	Low-level output voltage	$V_{CC} = MIN,$ $V_{IL} = 0.8 V,$	$V_{IH} = 2 V$, $I_{OL} = 40 \text{ mA}$			0.2	0.4		0.2	0.45	٧	
Voic	Output alamp valtage	$V_{CC} = 5 V$,	I _O = 40 mA,	T _A = 25°C		6.1	6.5		6.1	6.5	V	
VOK C	Output clamp voltage	$V_{CC} = MAX$,	$I_{O} = -40 \text{ mA},$	T _A = 25°C		-1.1	-1.5		-1.1	-1.5	V	
	Off-state open collector output current	V _{CC} = MAX	V _{OH} = 12 V	T _A = 25°C		1	100				μΑ	
lo (m				T _A = 125°C			200					
IO(off)			V _{OH} = 5.25 V	T _A = 25°C					1	100		
			VOH = 3.23 V	T _A = 70°C						200		
t _l	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 5.5 V				1			1	mA	
Ιн	High-level input current	$V_{CC} = MAX$,	V _I = 2.4 V				40			40	μΑ	
I _I L	Low-level input current	$V_{CC} = MAX$,	V _I = 0.4 V			-1.1	-1.6		-1.1	-1.6	mA	
los	Short-circuit output current§	V _{CC} = MAX,	V _O = 0,	T _A = 25°C	-40	-90	-120	-40	-90	-120	mA	
loo	Supply current	All inputs at 0	V, No load,	$V_{CC} = MAX$		37	50		37	50	mA	
Icc	(both drivers)	T _A = 25°C		$V_{CC} = 7 V$		47	65		47	70	111/4	

[†] All parameters, with the exception of off-state open-collector output current, are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

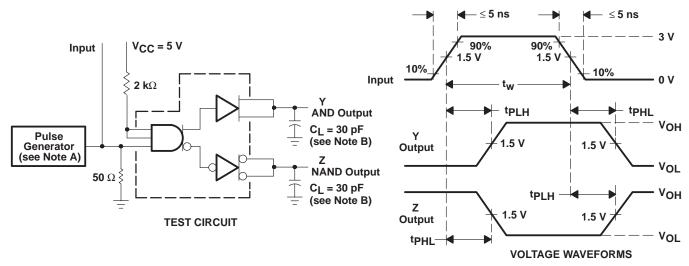
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST	S	N55114		S	UNIT		
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output	$C_L = 30 pF$,		15	20		15	30	ns
tPHL	Propagation delay time, high- to low-level output	See Figure 1		11	20		11	30	ns

 $^{^{\}ddagger}$ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.

[§] Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

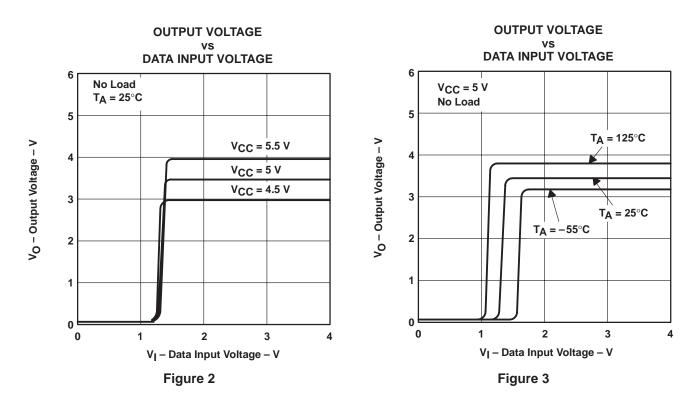
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $Z_0 = 500 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W \leq 100 \text{ ns}$.
 - B. C_I includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

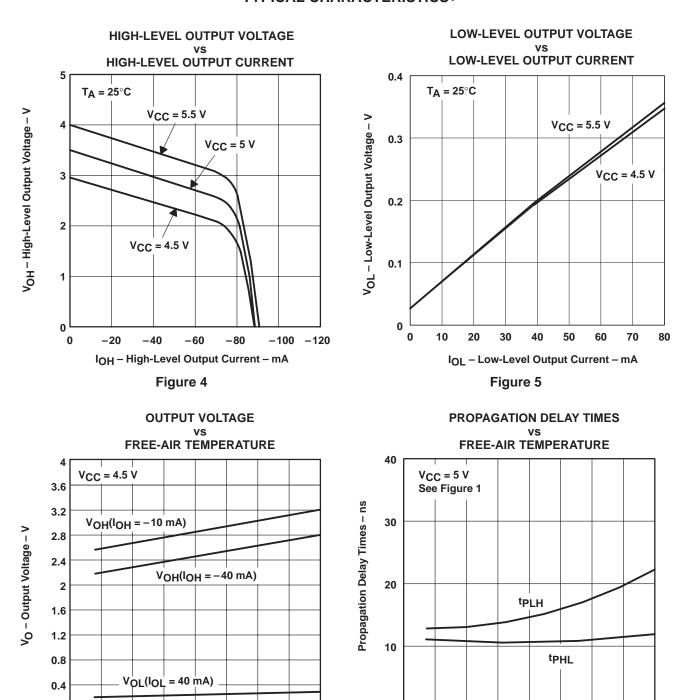
TYPICAL CHARACTERISTICS†



[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. These parameters were measured with the active pullup connected to the sink output.



TYPICAL CHARACTERISTICS[†]



-75 -50

0

-25

50

75

100

125

25

 T_A – Free-Air Temperature – $^{\circ}$ C

Figure 7



-75 -50

-25

0

25

 T_A – Free-Air Temperature – $^{\circ}$ C

Figure 6

50

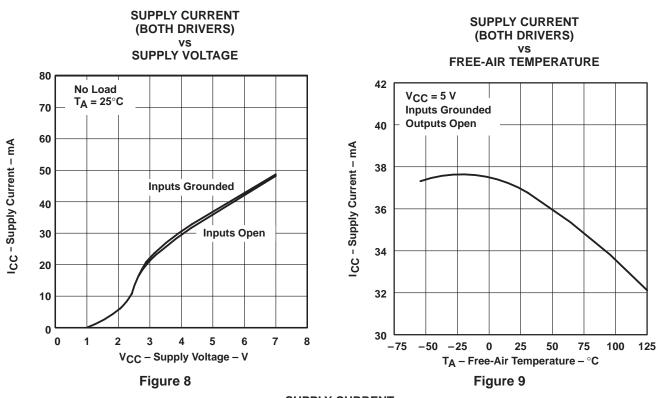
75

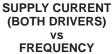
100

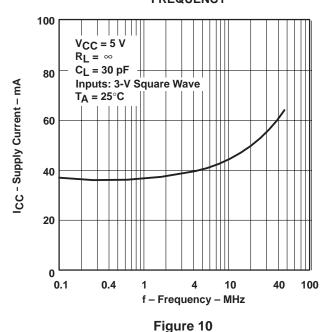
125

[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

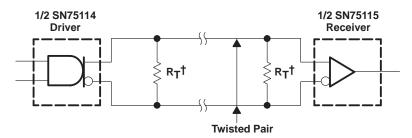






† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



 $^{^{\}dagger}$ R_T = Z_O. A capacitor can be connected in series with R_T to reduce power dissipation.

Figure 11. Basic Party-Line or Data-Bus Differential Data Transmission

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PACKAGE OPTION ADDENDUM



ti.com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
5962-88744022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8874402EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8874402FA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/10403BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN55114J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN75114D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75114DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75114DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75114DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75114DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75114DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75114J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75114N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75114NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ55114FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55114J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55114W	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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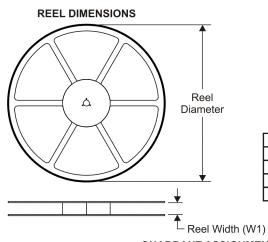
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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

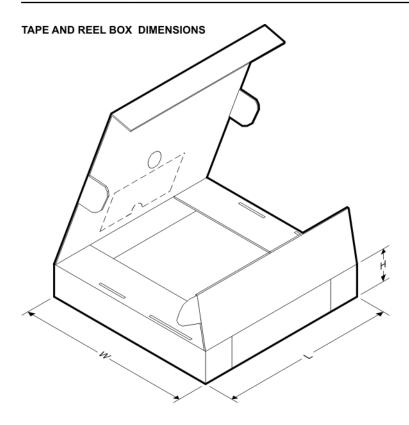
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ı	SN75114DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75114DR	SOIC	D	16	2500	333.2	345.9	28.6

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

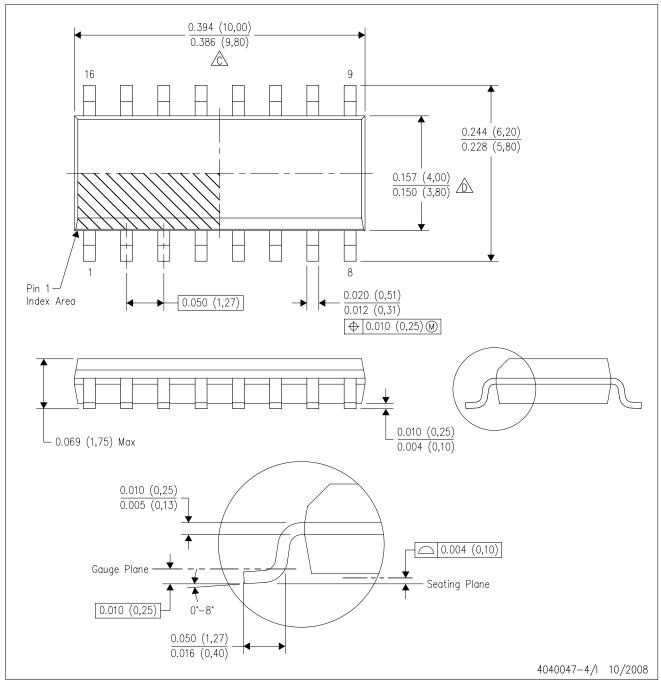


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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