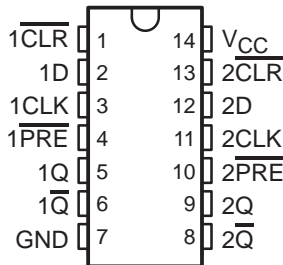


SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

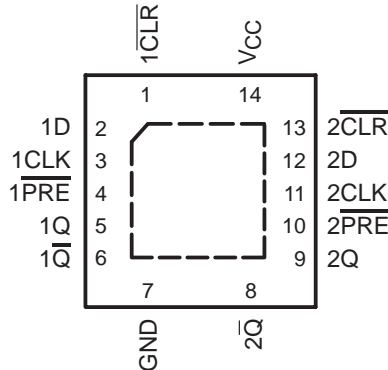
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <math><0.8\text{ V}</math> at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

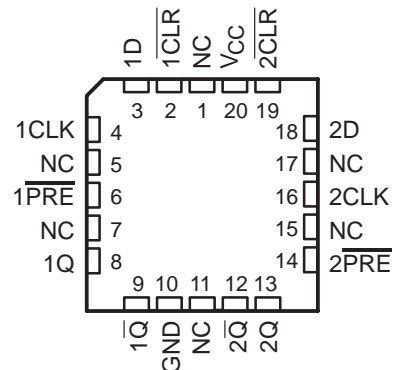
SN54LVC74A . . . J OR W PACKAGE
SN74LVC74A . . . D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC74A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN54LVC74A dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC74A dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC74ARGYR	
	SOIC – D	Tube of 50	SN74LVC74AD	LVC74A
		Reel of 2500	SN74LVC74ADR	
		Reel of 250	SN74LVC74ADT	
	SOP – NS	Reel of 2000	SN74LVC74ANSR	LCV74A
	SSOP – DB	Reel of 2000	SN74LVC74ADBR	LC74A
–55°C to 125°C	TSSOP – PW	Tube of 90	SN74LVC74APW	LC74A
		Reel of 2000	SN74LVC74APWR	
		Reel of 250	SN74LVC74APWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC74AJ	SNJ54LVC74AJ
	CFP – W	Tube of 150	SNJ54LVC74AW	SNJ54LVC74AW
	LCCC – FK	Tube of 55	SNJ54LVC74AFK	SNJ54LVC74AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply-voltage range, V_{CC}	–0.5 V to 6.5 V
Input-voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output-voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

		SN54LVC74A		SN74LVC74A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5	1.5	
V_{IH}	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V			1.7	
		$V_{CC} = 2.7$ V to 3.6 V	2	2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V			0.7	
		$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65$ V			–4	mA
		$V_{CC} = 2.3$ V			–8	
		$V_{CC} = 2.7$ V		–12	–12	
		$V_{CC} = 3$ V		–24	–24	
I_{OL}	Low-level output current	$V_{CC} = 1.65$ V			4	mA
		$V_{CC} = 2.3$ V			8	
		$V_{CC} = 2.7$ V		12	12	
		$V_{CC} = 3$ V		24	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC74A			SN74LVC74A			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V				V _{CC} -0.2			V	
		2.7 V to 3.6 V	V _{CC} -0.2							
	I _{OH} = -4 mA	1.65 V			1.2					
	I _{OH} = -8 mA	2.3 V			1.7					
	I _{OH} = -12 mA	2.7 V	2.2		2.2					
		3 V	2.4		2.4					
I _{OH} = -24 mA	3 V	2.2		2.2						
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V	
		2.7 V to 3.6 V			0.2					
	I _{OL} = 4 mA	1.65 V				0.45				
	I _{OL} = 8 mA	2.3 V				0.7				
	I _{OL} = 12 mA	2.7 V			0.4		0.4			
		3 V			0.55		0.55			
I _I	V _I = 5.5 V or GND	3.6 V			±5			±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10			10	μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500			500	μA	
C _i	V _I = V _{CC} or GND	3.3 V			5			5	pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVC74A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		83		100	MHz
t _w	Pulse duration	PRE or CLR low		3.3	3.3	ns
		CLK high or low		3.3	3.3	
t _{su}	Setup time before CLK↑	Data		3.4	3	ns
		PRE or CLR inactive		2.2	2	
t _h	Hold time, data after CLK↑	1		1		ns



SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN74LVC74A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		83		83		83		100		MHz
t _w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4.1		3.3		3.3		3.3		ns
		CLK high or low	4.1		3.3		3.3		3.3		
t _{su}	Setup time before CLK↑	Data	3.6		2.3		3.4		3		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2.7		1.9		2.2		2		
t _h	Hold time, data after CLK↑		1		1		1		0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC74A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			83		100		MHz
t _{pd}	CLK	Q or $\overline{\text{Q}}$	6		1	5.2	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		6.4		1	5.4	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC74A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			83		83		83		100		MHz
t _{pd}	CLK	Q or $\overline{\text{Q}}$	1	7.1	1	4.4	1	6	1	5.2	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		1	6.9	1	4.6	1	6.4	1	5.4	
t _{sk(o)}									1	ns	

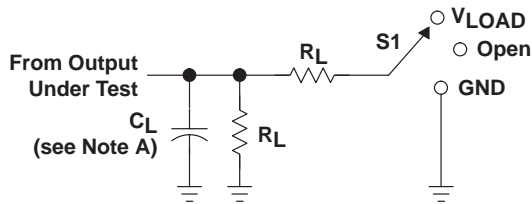
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT	
		TYP	TYP	TYP		
C _{pd}	Power dissipation capacitance per flip-flop	f = 10 MHz	24	24	26	pF

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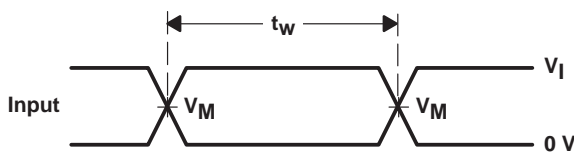
PARAMETER MEASUREMENT INFORMATION



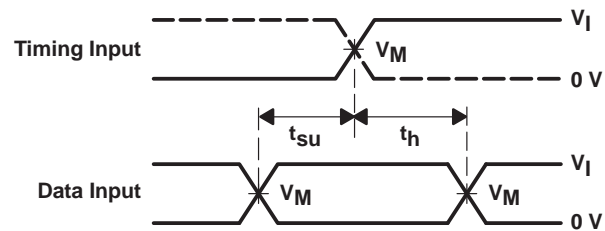
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

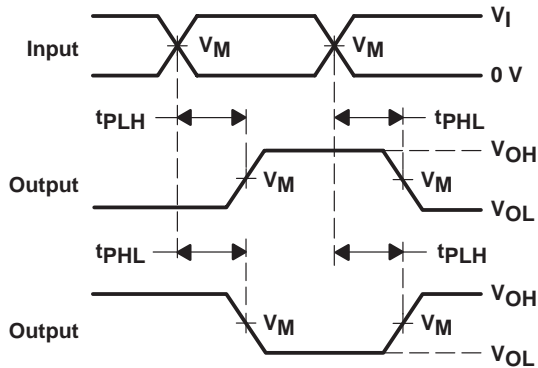
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



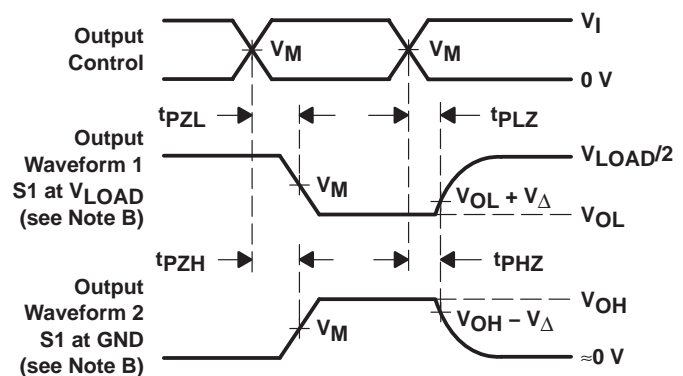
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

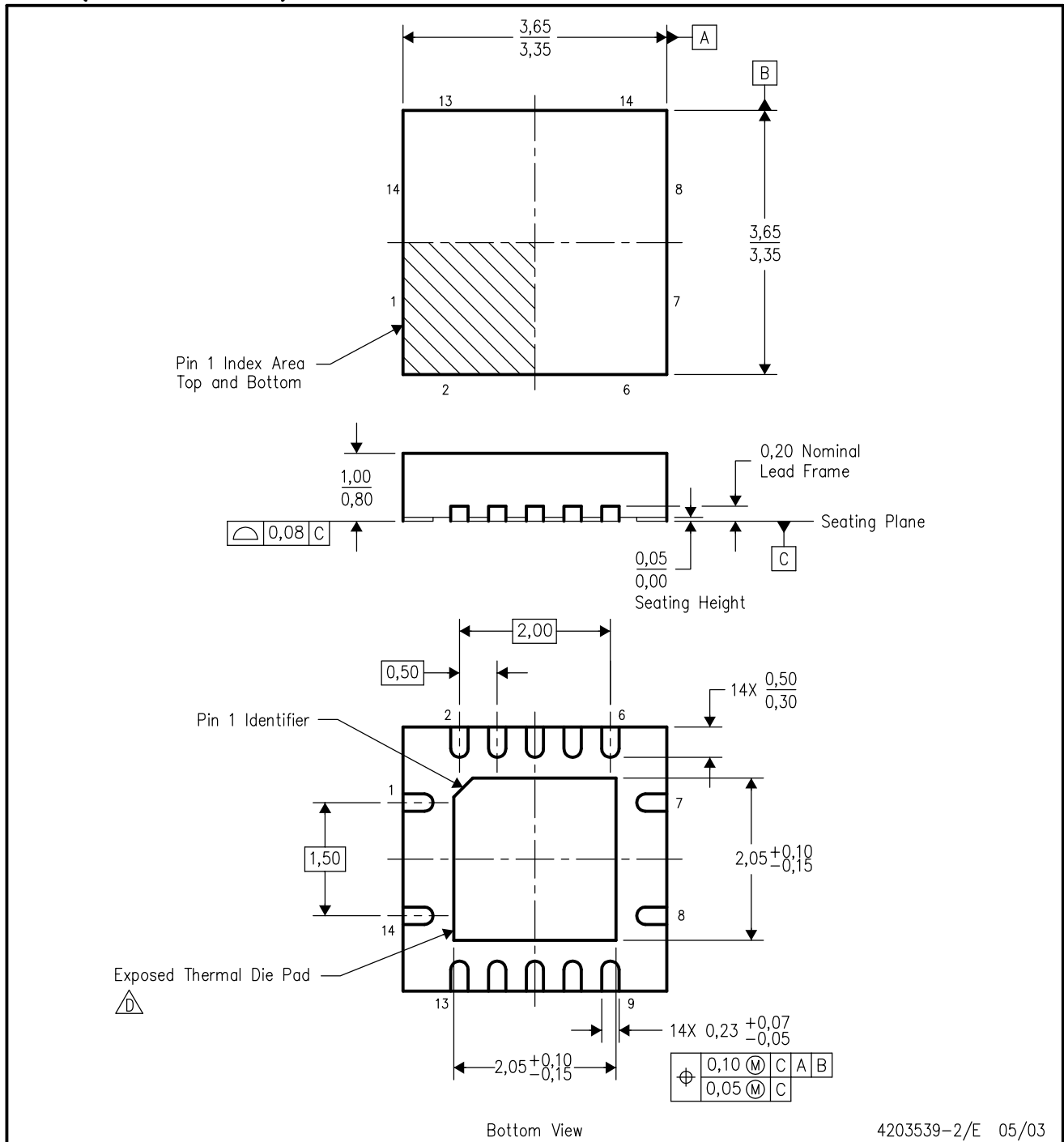
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK

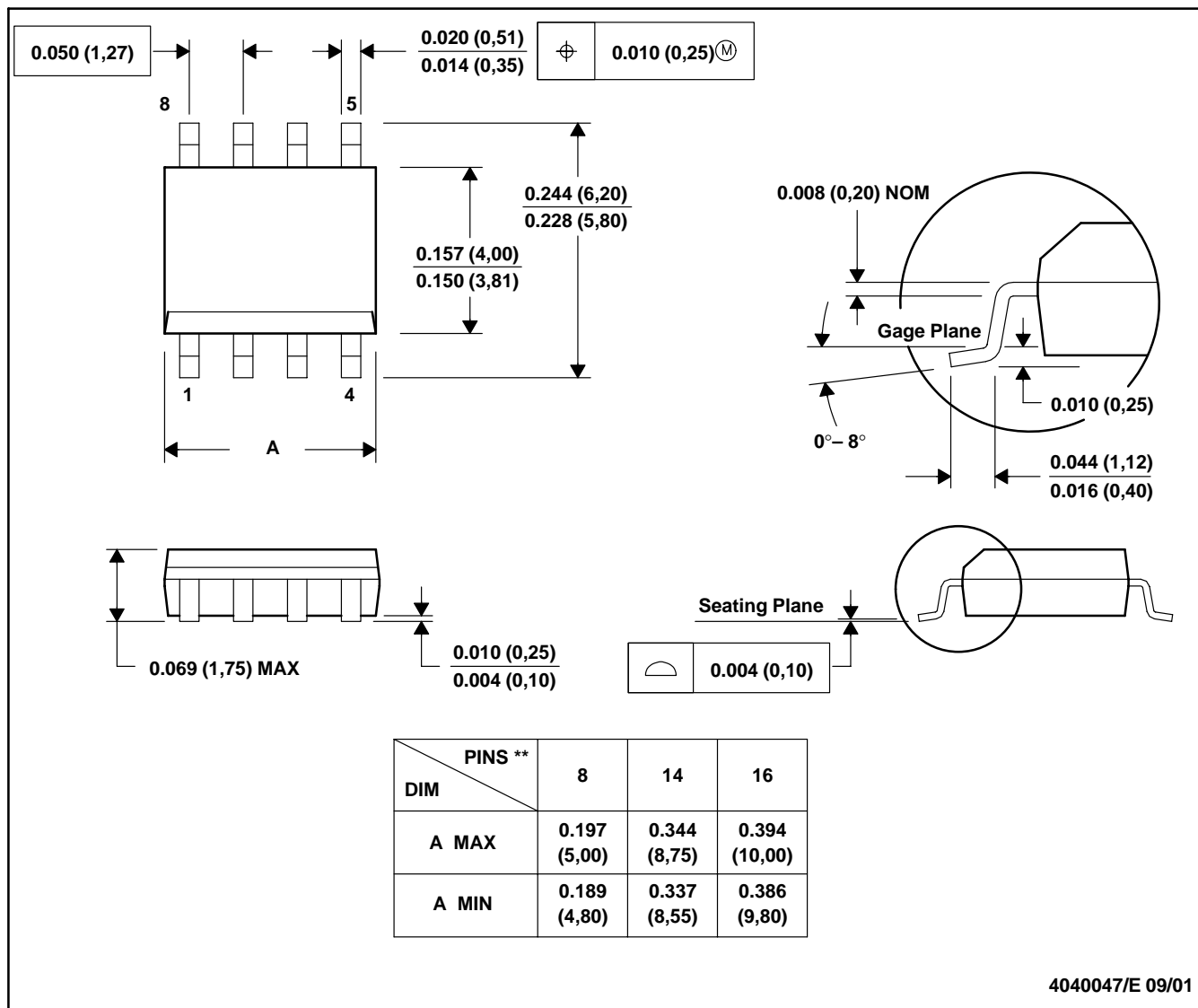


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - $\triangle D$ The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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