- **Operating Range 2-V to 5.5-V V_{CC}**
- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**

- **Same Pinouts as 'AHC00**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54AHC132 . . . J OR W PACKAGE
SN74AHC132 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)

```
1A  [ 1      14 ] V_CC
1B  [ 2      13 ] 4B
1Y  [ 3      12 ] 4A
2A  [ 4      11 ] 4Y
2B  [ 5      10 ] 3B
2Y  [ 6       9 ] 3A
GND [ 7       8 ] 3Y
```
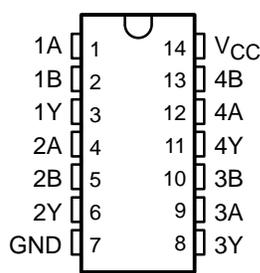
SN74AHC132 . . . RGY PACKAGE
(TOP VIEW)

```
         1A    V_CC
          1     14
1B [ 2           13 ] 4B
1Y [ 3           12 ] 4A
2A [ 4           11 ] 4Y
2B [ 5           10 ] 3B
2Y [ 6            9 ] 3A
          7     8
         GND    3Y
```
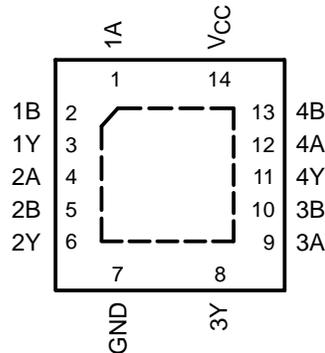
SN54AHC132 . . . FK PACKAGE
(TOP VIEW)

```
         1B 1A NC V_CC 4B
          3  2  1  20 19
1Y [ 4               18 ] 4A
NC [ 5               17 ] NC
2A [ 6               16 ] 4Y
NC [ 7               15 ] NC
2B [ 8               14 ] 3B
          9 10 11 12 13
         2Y GND NC 3Y 3A
```
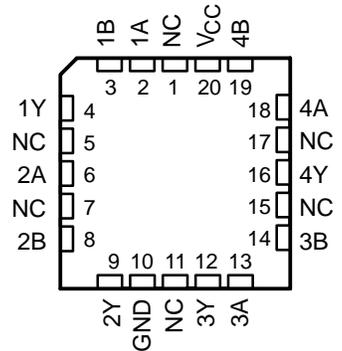
NC – No internal connection

description/ordering information

The 'AHC132 devices are quadruple positive-NAND gates designed for 2-V to 5.5-V V_{CC} operation.

These devices perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC132RGYR	HA132
	PDIP – N	Tube	SN74AHC132N	SN74AHC132N
	SOIC – D	Tube	SN74AHC132D	AHC132
		Tape and reel	SN74AHC132DR	
	SOP – NS	Tape and reel	SN74AHC132NSR	AHC132
	SSOP – DB	Tape and reel	SN74AHC132DBR	HA132
	TSSOP – PW	Tape and reel	SN74AHC132PWR	HA132
	TVSOP – DGV	Tape and reel	SN74AHC132DGVR	HA132
−55°C to 125°C	CDIP – J	Tube	SNJ54AHC132J	SNJ54AHC132J
	CFP – W	Tube	SNJ54AHC132W	SNJ54AHC132W
	LCCC – FK	Tube	SNJ54AHC132FK	SNJ54AHC132FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)
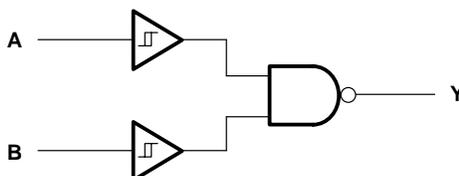
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	–20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			SN54AHC132		SN74AHC132		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC132		SN74AHC132		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		3 V	1.2		2.2	1.2	2.2	1.2	2.2	V
		4.5 V	1.75		3.15	1.75	3.15	1.75	3.15	
		5.5 V	2.15		3.85	2.15	3.85	2.15	3.85	
$V_{T−}$ Negative-going input threshold voltage		3 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		4.5 V	1.35		2.75	1.35	2.75	1.35	2.75	
		5.5 V	1.65		3.35	1.65	3.35	1.65	3.35	
ΔV_T Hysteresis ($V_{T+} − V_{T−}$)		3 V	0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V_{OH}	I_{OH} = −50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	µA
C_i	V_I = V_{CC} or GND	5 V		1.9	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

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switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC132		SN74AHC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		5.6*	11.9*	1*	14*	1	14	ns
t_{PHL}					5.6*	11.9*	1*	14*	1	14	
t_{PLH}	A or B	Y	C_L = 50 pF		7.6	15.4	1	17.5	1	17.5	ns
t_{PHL}					7.6	15.4	1	17.5	1	17.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC132		SN74AHC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		3.9*	7.7*	1*	9*	1	9	ns
t_{PHL}					3.9*	7.7*	1*	9*	1	9	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	9.7	1	11	1	11	ns
t_{PHL}					5.3	9.7	1	11	1	11	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

| PARAMETER		SN74AHC132			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.45	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.35	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	11	pF

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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