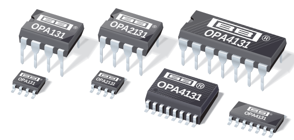
Burr-Brown Products
from Texas Instruments

OPA131
OPA2131
OPA4131



SBOS040A – NOVEMBER 1994 – REVISED DECEMBER 2002

General-Purpose
FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

- **FET INPUT: I_B = 50pA max**
- **LOW OFFSET VOLTAGE: 750μV max**
- **WIDE SUPPLY RANGE: ±4.5V to ±18V**
- **SLEW RATE: 10V/μs**
- **WIDE BANDWIDTH: 4MHz**
- **EXCELLENT CAPACITIVE LOAD DRIVE**
- **SINGLE, DUAL, QUAD VERSIONS**

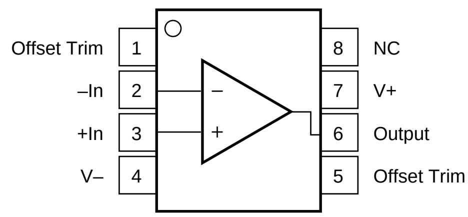
DESCRIPTION

The OPA131 series of FET-input op amps provides high performance at low cost. Single, dual, and quad versions in industry-standard pinouts allow cost-effective design options.

The OPA131 series offers excellent general-purpose performance, including low offset voltage, drift, and good dynamic characteristics.

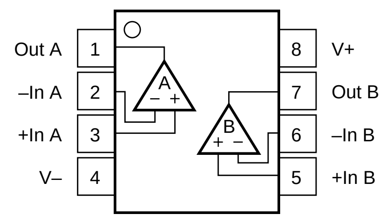
Single, dual, and quad versions are available in DIP and SO packages. Performance grades include commercial and industrial temperature ranges.

OPA131



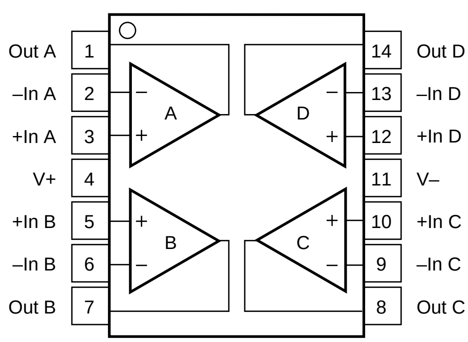
DIP-8, SO-8

OPA2131



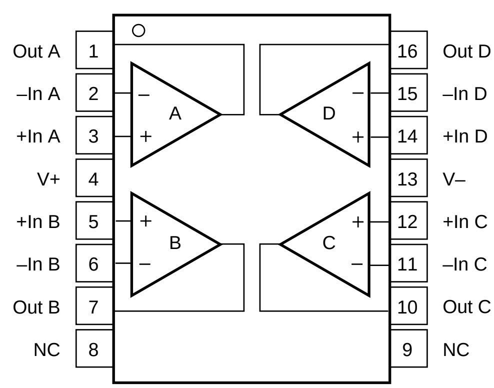
DIP-8, SO-8

OPA4131



DIP-14, SO-14

OPA4131



SOL-16

NC = No Connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Input Voltage	(V–) – 0.7V to (V+) + 0.7V
Output Short-Circuit[2]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Single						
OPA131	SO-8	D	–40°C to +85°C	OPA131UJ	OPA131UJ	Rails, 100
"	"	"	"	"	OPA131UJ/2K5	Tape and Reel, 2500
OPA131	SO-8	D	–40°C to +85°C	OPA131UA	OPA131UA	Rails, 100
"	"	"	"	"	OPA131UA/2K5	Tape and Reel, 2500
OPA131	SO-8	D	–40°C to +85°C	OPA131U	OPA131U	Rails, 100
"	"	"	"	"	OPA131U/2K5	Tape and Reel, 2500
Dual						
OPA2131	SO-8	D	–40°C to +85°C	OPA2131UJ	OPA2131UJ	Rails, 100
"	"	"	"	"	OPA2131UJ/2K5	Tape and Reel, 2500
OPA2131	SO-8	D	–40°C to +85°C	OPA2131UA	OPA2131UA	Rails, 100
"	"	"	"	"	OPA2131UA/2K5	Tape and Reel, 2500
Quad						
OPA4131	DIP-14	N	–40°C to +85°C	OPA4131PJ	OPA4131PJ	Rails, 25
"	"	"	"	OPA4131PA	OPA4131PA	Rails, 25
OPA4131	SOL-16	DW	–40°C to +85°C	OPA4131UA	OPA4131UA	Rails, 48
"	"	"	"	"	OPA4131UA/1K	Tape and Reel, 1000
OPA4131	SOL-14	D	–40°C to +85°C	OPA4131NJ	OPA4131NJ	Rails, 58
"	"	"	"	OPA4131NA	OPA4131NA	Rails, 58

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

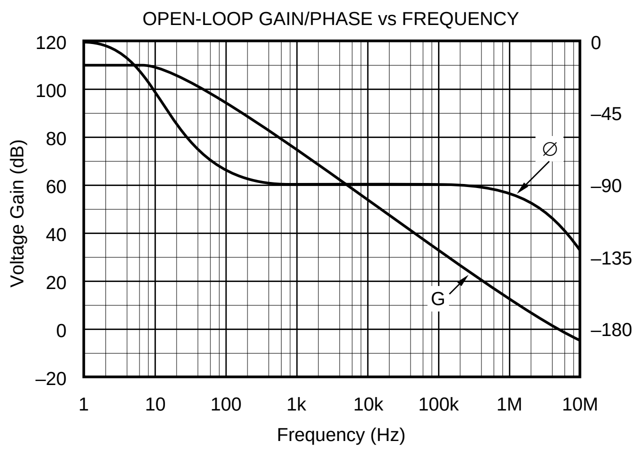
		OPA131UA OPA2131UA OPA4131PA, UA, NA			OPA131UJ OPA2131UJ OPA4131PJ, NJ			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			±0.2	±1		*	±1.5	mV
OPA131U model only			±0.2	0.75				mV
vs Temperature(1)	Operating Temperature Range		±2	±10		*	*	μV/°C
vs Power Supply	V_S = ±4.5V to ±18V		50	200		*	*	μV/V
OPA131U model only			50	100				μV/V
INPUT BIAS CURRENT(2)								
Input Bias Current	V_{CM} = 0V		+5	±50		*	*	pA
vs Temperature			See Typical Characteristic			*		
Input Offset Current	V_{CM} = 0V		±1	±50		*	*	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 10Hz			21			*		nV/√Hz
f = 100Hz			16			*		nV/√Hz
f = 1kHz			15			*		nV/√Hz
f = 10kHz			15			*		nV/√Hz
Current Noise Density, f = 1kHz			3			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		(V–) + 3		(V+) – 1	*		*	V
Common-Mode Rejection	V_{CM} = –12V to +14V	70	80		*	*		dB
OPA131U model only		80	86					dB
INPUT IMPEDANCE								
Differential			$10^{10} \parallel 1$			*		Ω ∥ pF
Common-Mode	V_{CM} = 0V		$10^{12} \parallel 3$			*		Ω ∥ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = –12V to +12V	94	110		*	*		dB
OPA131U model only		100	110					dB
FREQUENCY RESPONSE								
Gain-Bandwidth Product			4			*		MHz
Slew Rate			10			*		V/μs
Settling Time 0.1%	G = –1, 10V Step, C_L = 100pF		1.5			*		μs
0.01%	G = –1, 10V Step, C_L = 100pF		2			*		μs
Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5Vrms		0.0008			*		%
OUTPUT								
Voltage Output, Positive		(V+) – 3	(V+) – 2.5		*	*		V
Negative		(V–) + 3	(V–) + 2.5		*	*		V
Short-Circuit Current			±25			*		mA
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Quiescent Current (per amplifier)	I_O = 0		±1.5	±1.75		*	±2	mA
TEMPERATURE RANGE								
Operating Range		–55		+125	–55		+125	°C
Storage		–55		+125	*		*	°C
Thermal Resistance, θ_{JA}								
DIP-8			100			*		°C/W
SO-8			150			*		°C/W
DIP-14			80			*		°C/W
SO-14, SOL-16			110			*		°C/W

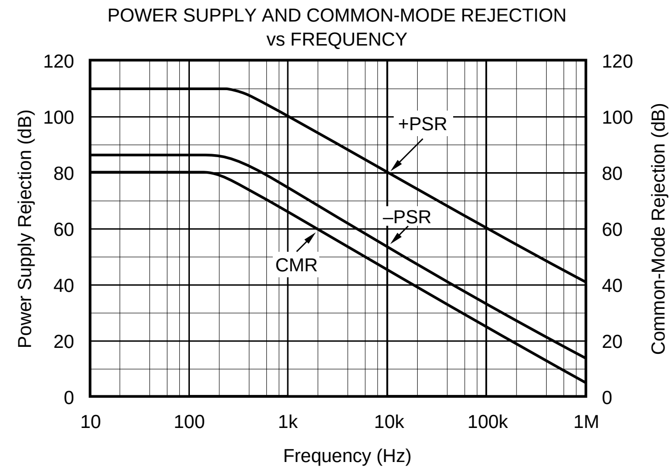
* Specifications same as OPA131UA.

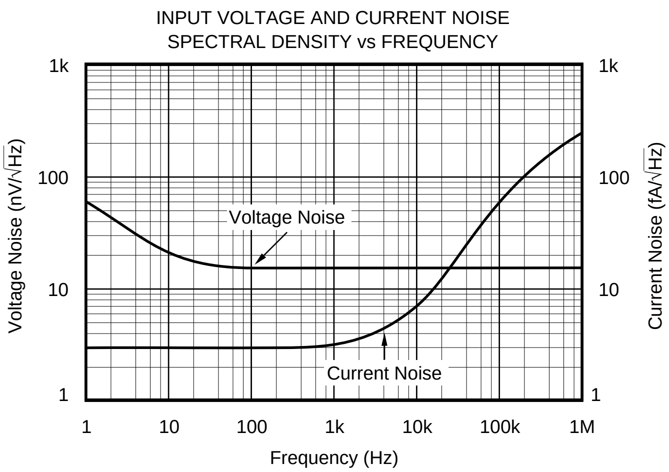
NOTES: (1) Ensured by wafer test. (2) High-speed test at T_J = 25°C.

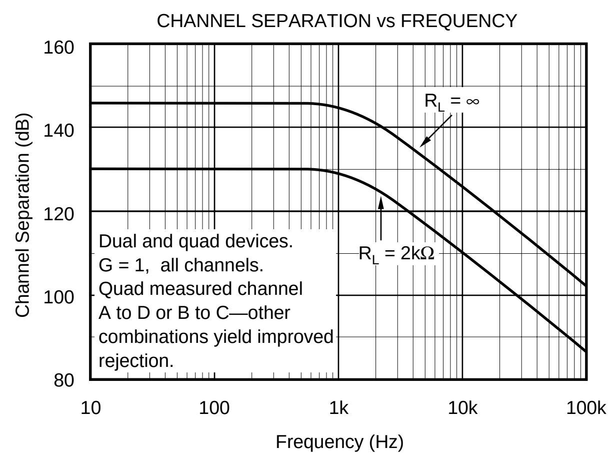
TYPICAL CHARACTERISTICS

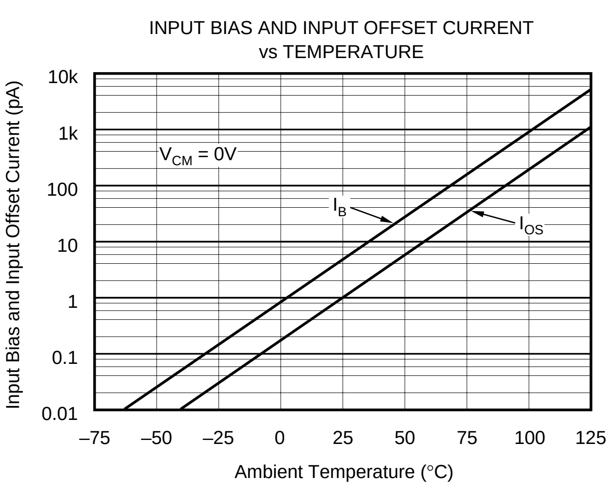
At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

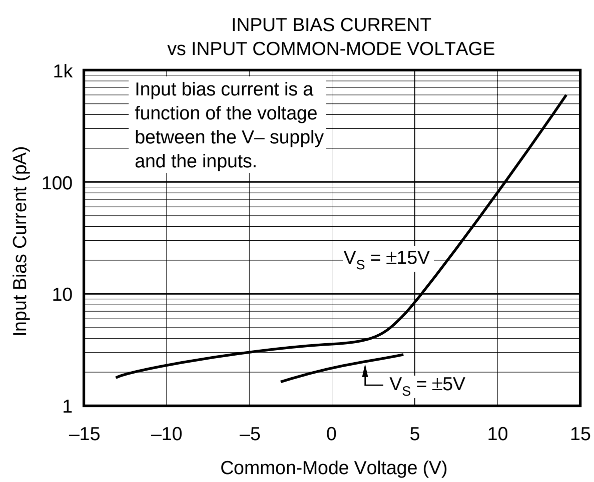








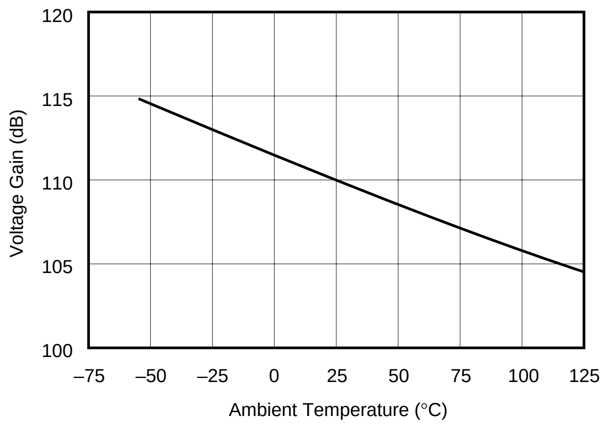




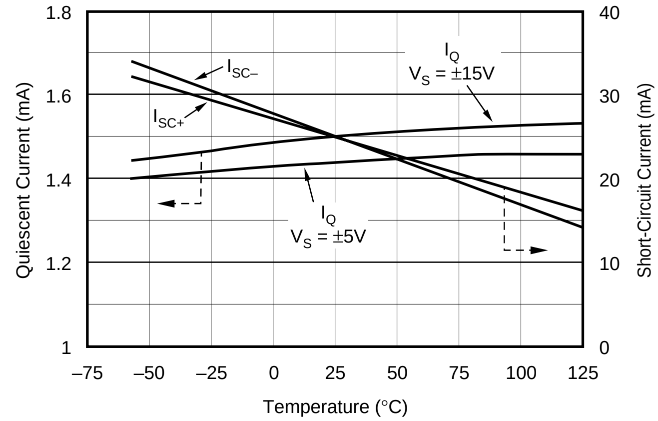
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25°C$, $V_S = ±15V$, and $R_L = 2kΩ$, unless otherwise noted.

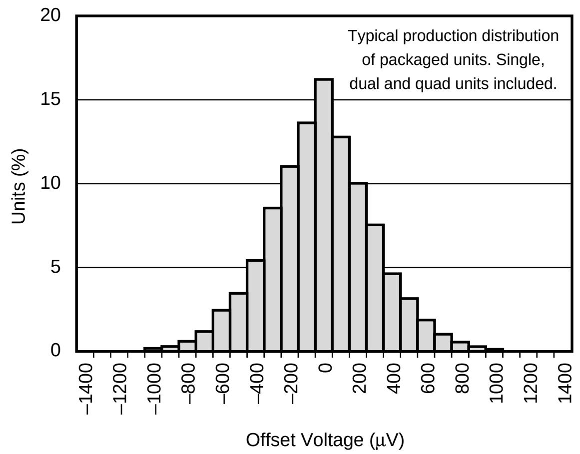
OPEN-LOOP GAIN vs TEMPERATURE



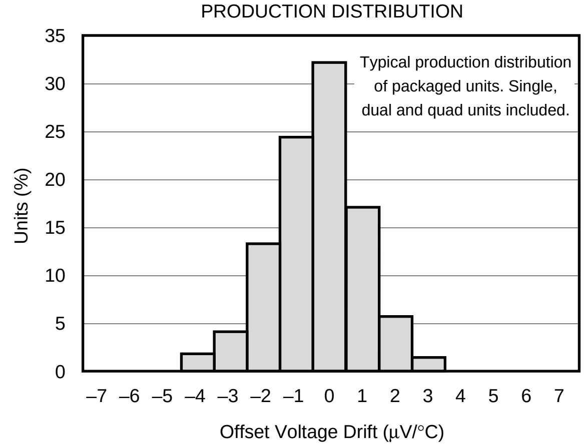
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



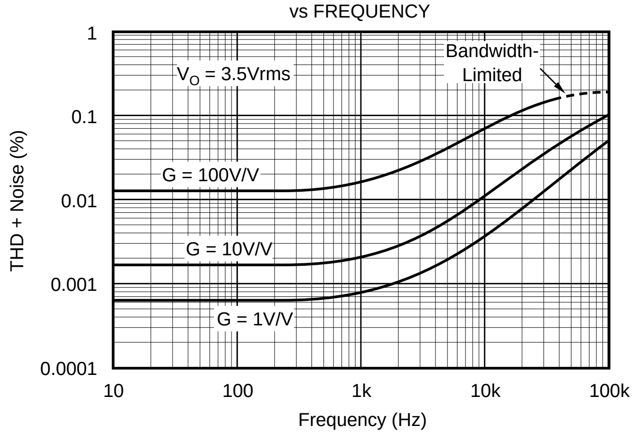
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



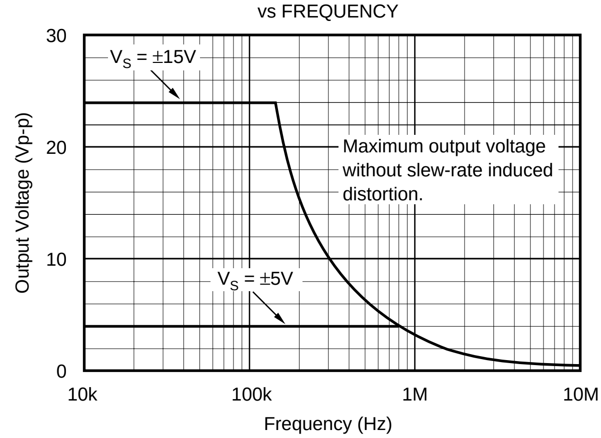
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



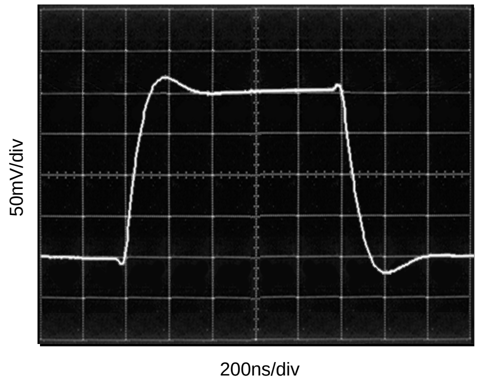
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



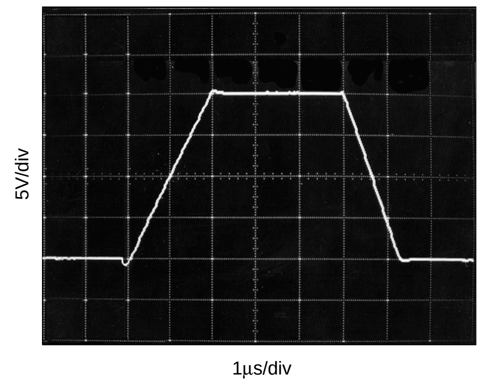
TYPICAL CHARACTERISTICS (Cont.)

At T_{CASE} = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

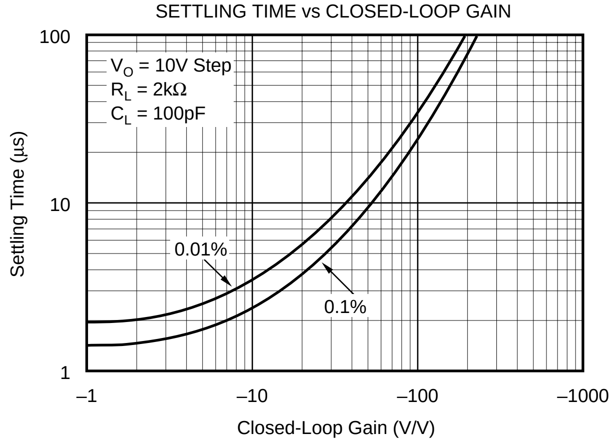
SMALL-SIGNAL STEP RESPONSE
G =1, C_L = 300pF



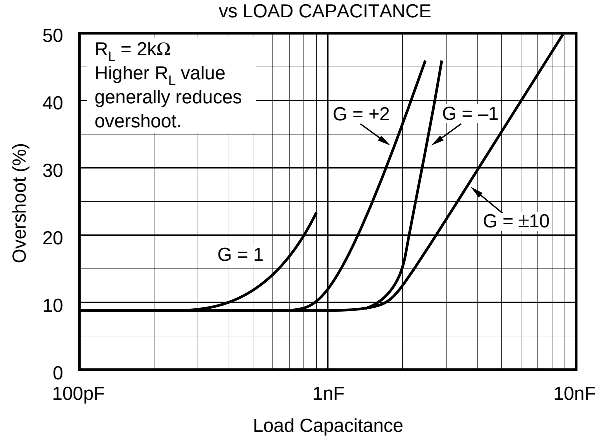
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 300pF



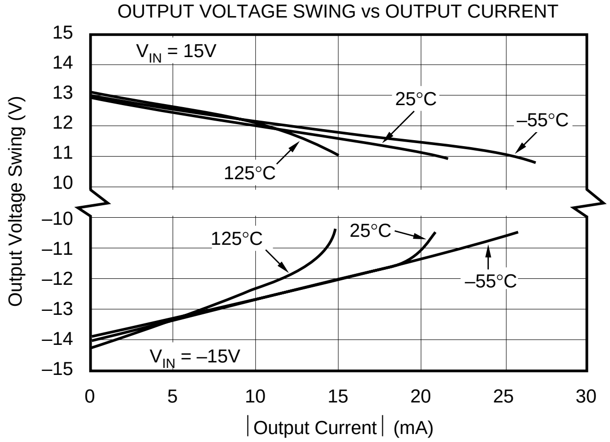
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

The OPA131 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10nF ceramic capacitors or larger.

The OPA131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control-loop applications. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

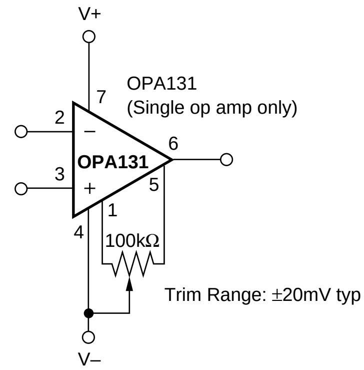


FIGURE 1. OPA131 Offset Voltage Trim Circuit.

OFFSET VOLTAGE TRIM

The OPA131 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not system offset or offset produced by the signal source.

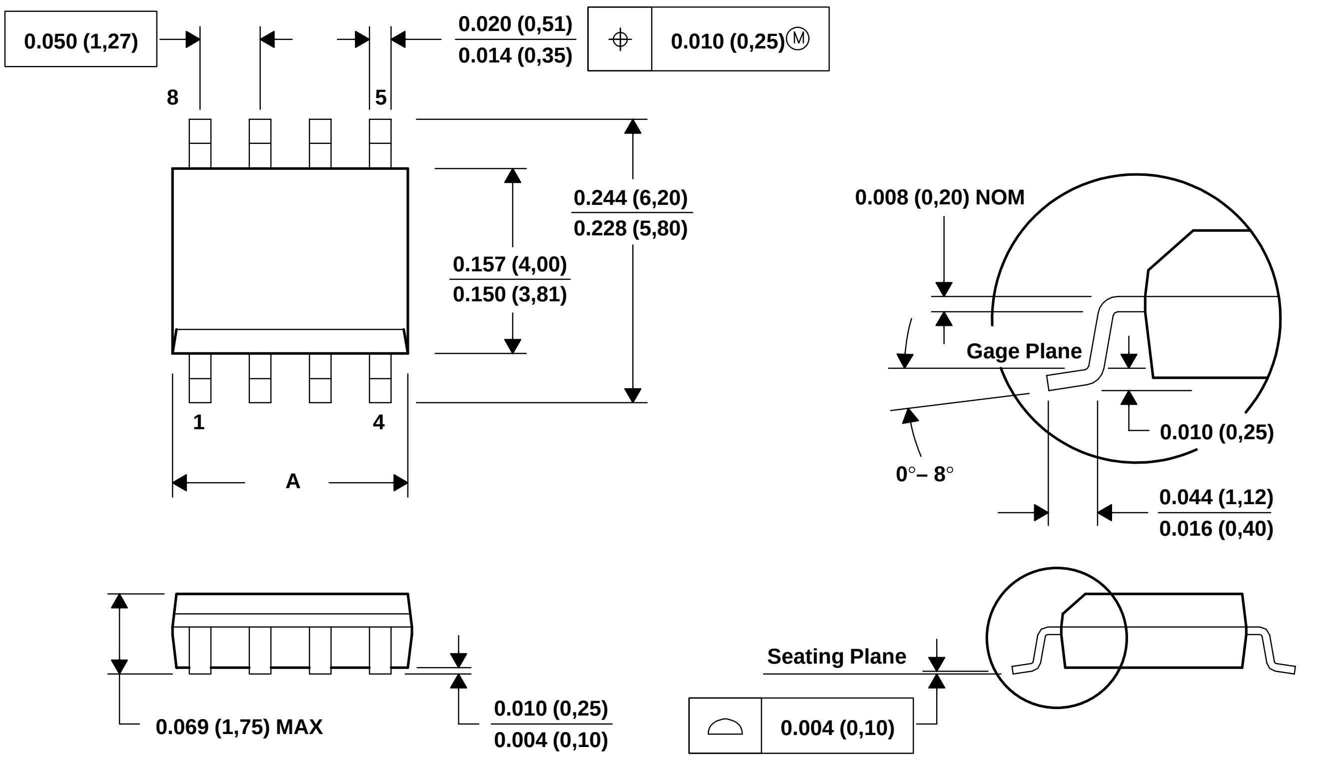
INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the typical characteristic “Input Bias Current vs Temperature.”

Input bias current also varies with common-mode voltage and power supply voltage. This variation is dependent on the voltage between the negative power supply and the common-mode input voltage. The effect is shown in the typical curve “Input Bias Current vs Common-Mode Voltage.”

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



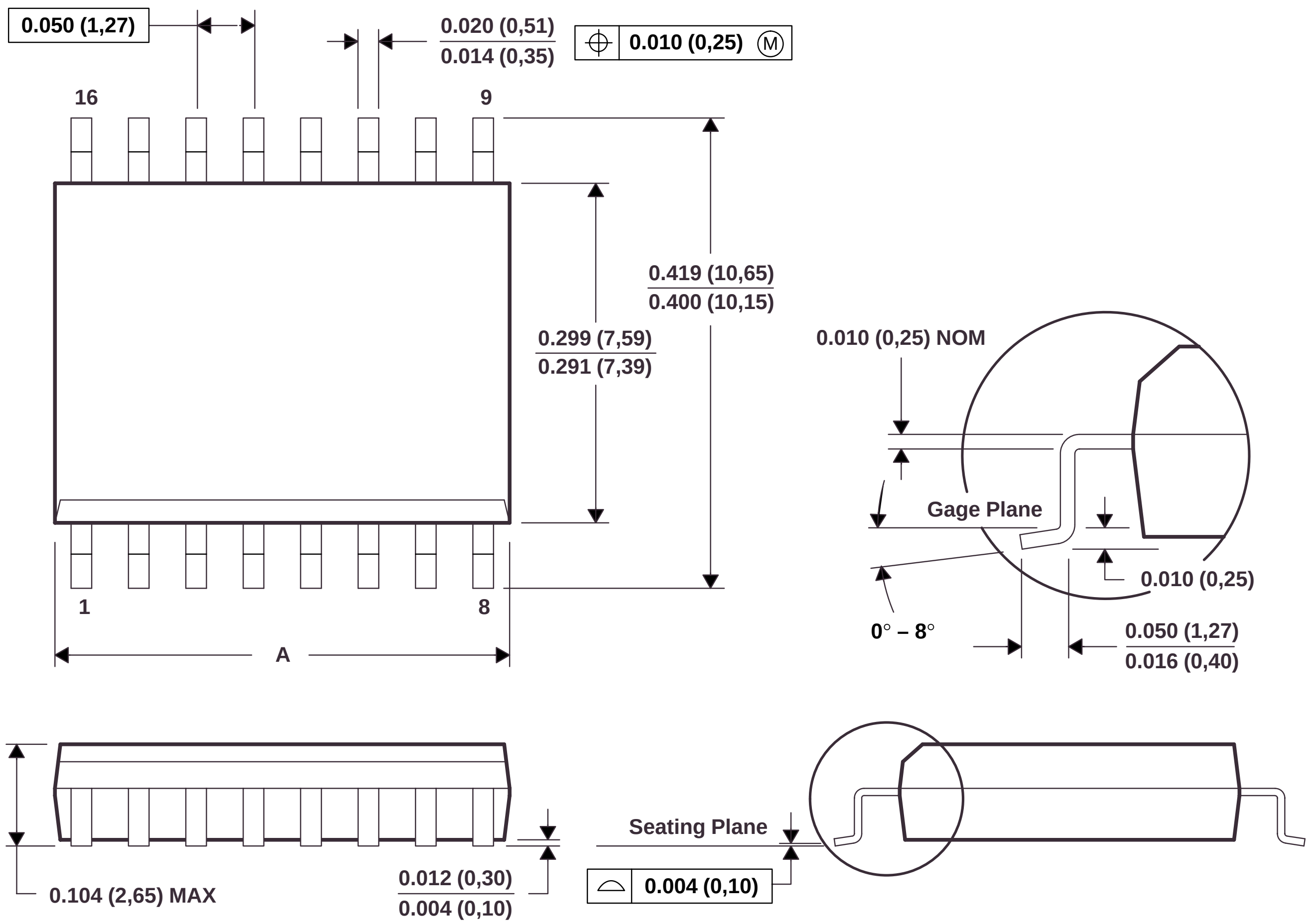
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000 / E 08/01

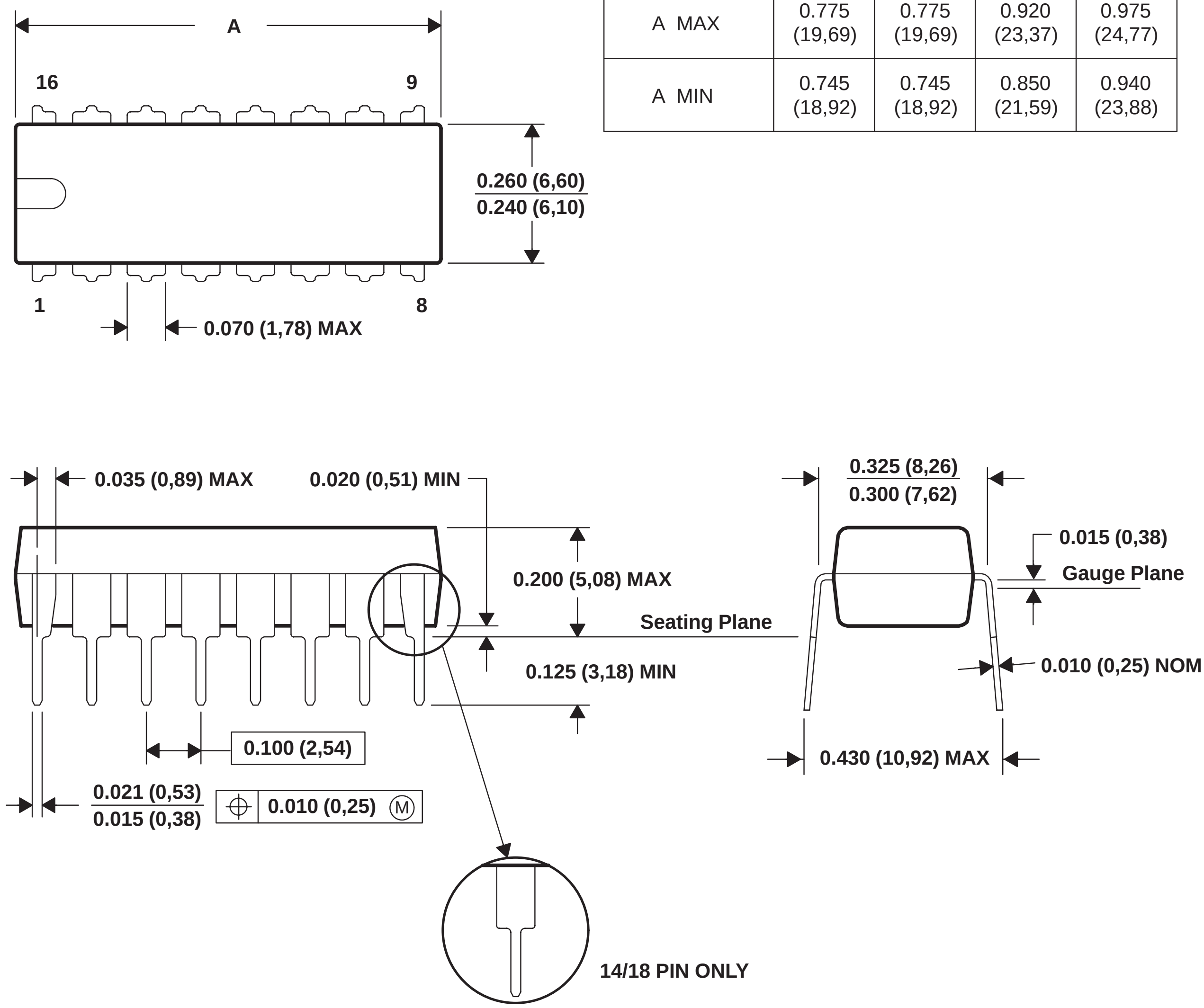
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

IMPORTANT NOTICE

Mailing Address:

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Post Office Box 655303
Dallas, Texas 75265