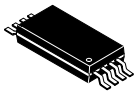
TEXAS INSTRUMENTS



SLUS509 – DECEMBER 2001

HIGH-PERFORMANCE BATTERY MONITOR WITH COLOUMB COUNTER AND FLASH MEMORY

FEATURES

- **Multifunction Monitoring Device Designed to Work With an Intelligent Host Controller**
  - **Provides State of Charge Information for Rechargeable Batteries**
  - **Enhances Charge Termination**
- **High Accuracy Coulometric Charge and Discharge Current Integration With Automatic Offset Compensation**
- **Differential Current Sense**
- **32 Bytes of General-Purpose RAM**
- **96 Bytes of Flash (Including 32 Bytes of Shadow Flash)**
- **8 Bytes of ID ROM**
- **Internal Temperature Sensor Eliminates Need for External Thermistor**
- **Multifunction Digital Output Port**
- **High-Accuracy Internal Timebase Eliminates External Crystal Oscillator**
- **Low Power Consumption**
  - **Operating : <95 μA**
  - **Sleep: <2 μA**
- **Single-Wire HDQ Serial Interface**
- **8-Lead TSSOP Package**

DESCRIPTION

The bq26200 is an advanced battery monitoring IC designed to accurately measure the charge and discharge currents in rechargeable battery packs. Intended for pack integration, the bq26200 contains all the necessary functions to form the basis of a comprehensive battery capacity management system in portable applications such as cellular phones, PDA's, or other portable products.

The bq26200 works with the host controller in the portable system to implement the battery management system. The host controller is responsible for interpreting the bq26200 data and communicating meaningful battery data to the end-user or power management system.

The bq26200 provides 64 bytes of general-purpose flash memory, 8 bytes of ID ROM and 32 bytes of flash backed RAM for data storage. The non-volatile memory can maintain formatted battery monitor information, identification codes, warranty information, or other critical battery parameters during periods when the battery is temporarily shorted or deeply discharged.

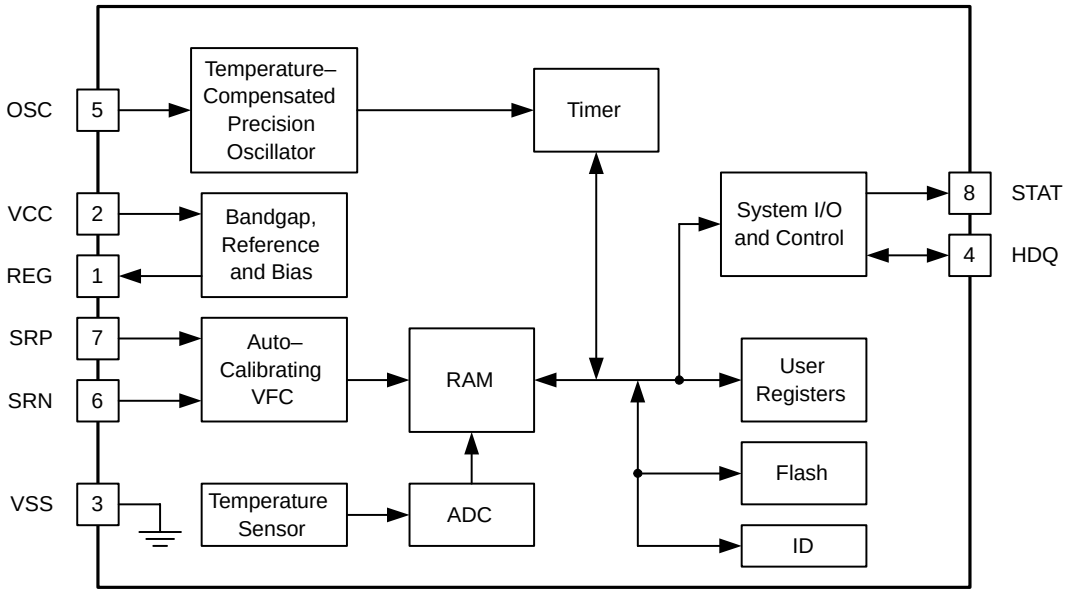
PW PACKAGE
(TOP VIEW)

AVAILABLE OPTIONS

T_A	MARKING	PACKAGE
		TSSOP (PW)
–20°C to 70°C	bq262	bq26200PW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



terminal functions

TERMINAL		I/O	DESCRIPTION
NAME	No.		
HDQ	4	I/O	Single-wire HDQ interface
OSC	5	O	Time base adjust for the oscillator
REG	1	O	Regulator output
SRN	6	I	Current sense input 2
SRP	7	I	Current sense input 1
STAT	8	O	Open-drain status output
VCC	2	I	Supply voltage
VSS	3	–	Ground

absolute maximum ratings over operating free–air temperature range (unless otherwise noted)†

Supply voltage (V_{CC} with respect to GND) . . . . . –0.3 to +7.0 V
Input voltage, SRP and SRN (all with respect to GND) . . . . . –0.3 V to V_{CC}+0.3 V
Output current (STAT) . . . . . 5 mA
Output current (REG) . . . . . 400 nA
Output current (HDQ) . . . . . 5 mA
Operating free-air temperature range, T_A . . . . . –20°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C
Lead temperature (soldering, 10 s) . . . . . 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
VCC	Supply voltage		2.8	5.5	V
T_A	Operating ambient temperature		–20	70	°C

dc electrical characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(OP)}$	Supply current	V_{CC} = 5.5 V, flash programming not active		88	120	µA
		V_{CC} = 4.3 V, flash programming not active		78	95	µA
$I_{(SLEEP)}$	Sleep current	2.8 V ≤ V_{CC} ≤ 4.3 V, flash programming not active		1	2	µA
$I_{CC(PROG)}$	Flash programming supply current	V_{CC} = 5.5 V		22	25	mA
$I_{CC(ERASE)}$	Flash erase supply current	V_{CC} = 5.5 V		14	25	mA
V_{OL}	Digital output low HDQ	I_{OL} = 1 mA			0.4	V
I_{OL}	Digital output low sink current				350	µA
V_{IL}	Digital input low HDQ pin				0.7	V
V_{IH}	Digital input high HDQ pin	V_{CC} < 4.2 V	1.7			V
		V_{CC} > 4.2 V	1.9			V
R_{SR}	SR input impedance	0.2 V < ($V_{(SRP)}$ – $V_{(SRN)}$) < V_{CC}	10			MΩ

ac electrical characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OR)}$	Power on reset delay	See Note 1			500	ms

NOTES: 1. Delay time after V_{CC} is at least 2.8 V before HDQ communication is attempted.

REG amplifier characteristics over recommended operating temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TH)}$	Regulator threshold		4.5	4.75	5.0	V

timer

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(OSC)}$	Oscillator current coefficient				10	ppm/Ω
$E_{(TMR)}$	Timer accuracy error	$R_{(OSC)}$ = 100 k (±0.1%), See Note 1	–3%		3%	

NOTES: 1. Timer accuracy is linearly proportional to the tolerance of $R_{(OSC)}$.

NOTES: 2. Variation of oscillator frequency due to change in $R_{(OSC)}$.

temperature register

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(RES)}$	Reported temperature resolution			1		°k
$E_{(T)}$	Reported temperature accuracy	V_{CC} = 3.6 V	–3		3	°K
	Reported temperature drift			–2		°kV

VFC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(SR)}$	Input voltage: $V_{SRP} – V_{SRN}$		–100		100	mV
$G_{(VFC)}$	Charge/discharge gain	T_A = 25 °C, V_{CC} = 3.6	89.2	92.2	95.2	Hz/V
$G_{(VCC)}$	Supply voltage gain coefficient	–100 mV < ($V_{(SRP)} – V_{(SRN)}$) < 100 mV		0.45	0.86	%/V
$G_{(TCO)}$	Temperature gain coefficient	Slope (–20°C ≤ T_A ≤ 70°C)	–0.03		0.02	%/°C
		Total deviation (–20°C ≤ T_A ≤ 70°C)		–0.15%	0.56%	
		Slope (0°C ≤ T_A ≤ 50°C)	–0.03		0.03	%/°C
		Total deviation (0°C ≤ T_A ≤ 50°C)		0.06%	0.51%	
INL	Integrated non-linearity	–100 mV < ($V_{(SRP)} – V_{(SRN)}$) < 100 mV		0.2%	0.5%	
$V_{(COS)}$	Auto compensated offset	2.8 V ≤ Vcc ≤ 4.3 V, $R_{(OSC)}$ = 100 K (±1%)	–17.7		12.5	µV

flash memory

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention				5	Years
	Flash programming write-cycles		10,000			Cycles
$t_{(BYTEPROG)}$	Byte programming time				90	µs
$t_{(BLCKPROG)}$	RAM-to-flash block programming time	60 µs +30 µs/byte			1020	µs
$t_{(BLKERASE)}$	Block-erase time	60 µs +30 µs/byte			1020	µs

standard serial communication (HDQ) timing, See Figures 1 and 2.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(B)}$	Break timing		190			µs
$t_{(BR)}$	Break recovery time		40			µs
$t_{(CYCH)}$	Host bit window		190			µs
$t_{(HW1)}$	Host sends 1		32		50	µs
$t_{(HW0)}$	Host sends 0		100		145	µs
$t_{(RSPS)}$	bq26200 to host response		190		320	µs
$t_{(CYCD)}$	bq26200 bit window		190		250	µs
$t_{(start–detect)}$	See Note 1		5			ns
$t_{(DW1)}$	Sends 1	bq26200	32		50	µs
$t_{(DW0)}$	Sends 0	bq26200	80		145	µs

NOTES: 1. The HDQ engine of the bq26220 inteprets a 5 ns or longer glitch on HDQ as a bit start. A sufficient number of glitches 5 ns or longer could result in incorrect data being written to the device. The HDQ line should be properly deglitched to ensure that this does not occur.

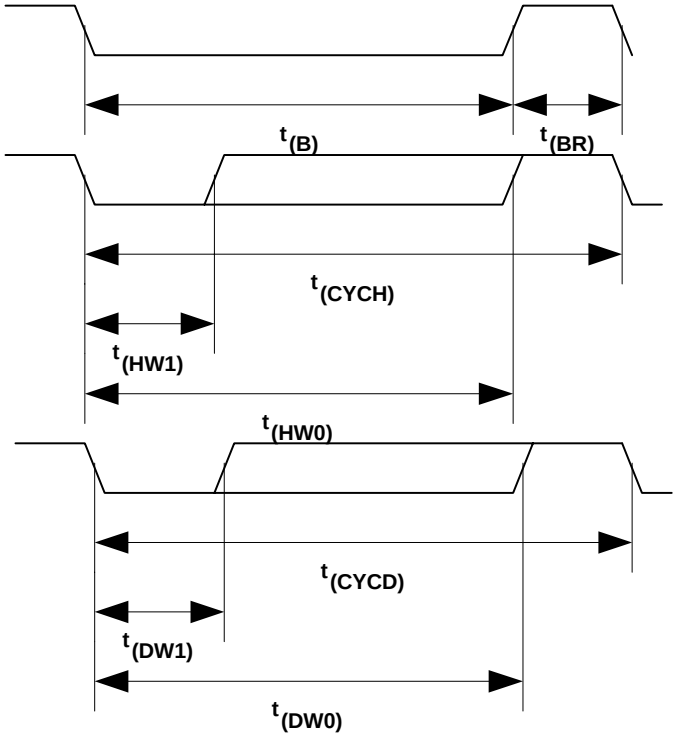


Figure 1. HDQ Timing Diagram

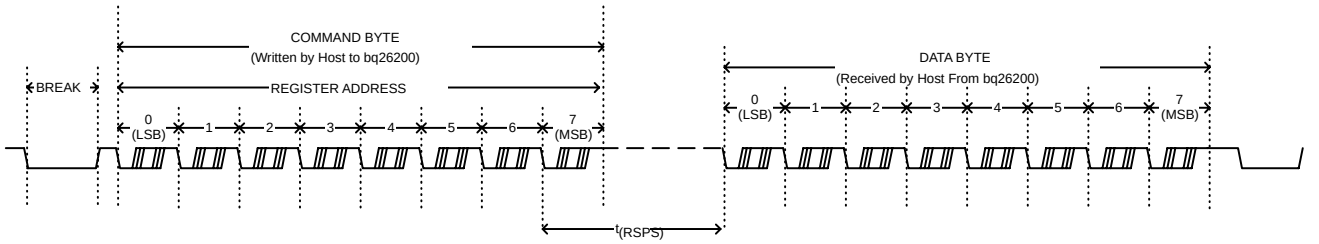


Figure 2. Typical Communication with the bq26200

detailed description

REG (regulator output)

REG is the output of the operational amplifier that drives an external pass N-channel JFET to provide an optional regulated supply. The supply is regulated at 4.75 V nominal.

HDQ (data input/output)

HDQ is a single-wire serial communications interface port. This bidirectional input/output communicates the register information to the host.

STAT (status output)

STAT is a general-purpose output port whose state is controlled via the HDQ serial communications interface.

SRP and SRN (current sense inputs)

The bq26200 interprets charge and discharge activity by monitoring and integrating the voltage drop, V_{SR}, across pins SRP and SRN. The SRP input connects to the sense resistor and the negative terminal of the battery. The SRN input connects to the sense resistor and the negative terminal of the pack. $V_{(SRP)} < V_{(SRN)}$ indicates discharge, and $V_{(SRP)} > V_{(SRN)}$ indicates charge.

OSC (time base adjust for the oscillator)

OSC is a current source that sets the internal time base by an external resistor.

APPLICATION INFORMATION

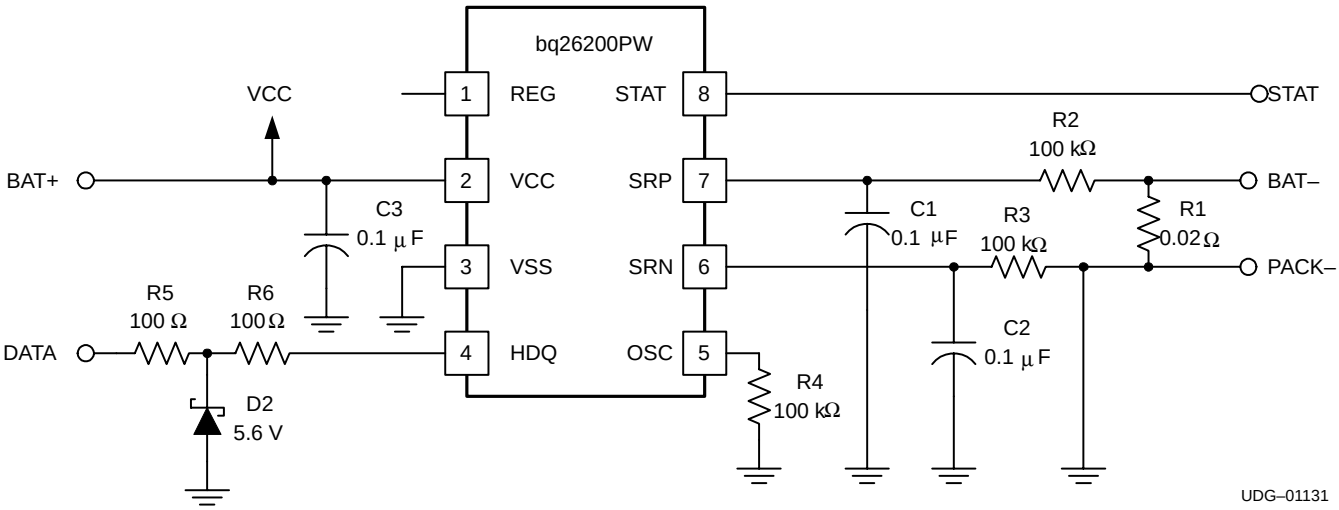


Figure 3. Typical Single-Cell Li-Ion/Li-Pol Application Diagram

functional description

The bq26200 measures the voltage drop across a low-value series-current sense-resistor between the SRP and SRN pins using a voltage to frequency converter. All data is placed into various internal counter and timer registers. Using information from the bq26200, the system host can determine the battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge currents. During pack storage periods, the use of an internal temperature sensor doubles the self-discharge count rate every 10°C above 25°C.The VFC offset is automatically compensated for in the charge and discharge counter registers.

Access to the registers and control of the bq26200 is accomplished via a single wire interface through a register mapped command protocol that includes placing the device in the low-power mode, hardware-register reset, programming flash from RAM, and transferring flash data to RAM.

The bq26200 can operate directly from a single Li-Ion cell or three or four nickel-chemistry cells for as long as V_{CC} is between 2.8 V and 5.5 V. To reduce cost in multicell applications, power to the bq26200 may be regulated using a low-cost external FET in conjunction with the REG pin.

REG output

The bq26200 can operate directly from three or four nickel-chemistry cells or a single Li-Ion cell as long as V_{CC} is between 2.8 V and 5.5 V. To facilitate the power supply requirements of the bq26200, the REG output is used in conjunction with an external low-threshold n-JFET when regulation from a higher source potential is required. The REG output remains active in sleep mode. For applications that do not need the REG output, operating current can be reduced by turning off the operational amplifier with the DISREG bit in the MODE/WOE register. For more details, refer to the *MODE/WOE register* section

APPLICATION INFORMATION

charge and discharge count operation

Table 1 shows the main counters and registers of the bq26200.

The bq26200 accumulates charge and discharge counts into two count registers: the charge count register (CCR) and the discharge count register (DCR). Charge and discharge counts are generated by sensing the voltage difference between SRP and SRN. The CCR or DCR independently counts, depending on the signal between pins SRP and SRN.

During discharge, the DCR and the discharge time counter (DTC) are active. If $(V_{(SRP)} – V_{(SRN))}$ is less than 0, indicating a discharge activity, the DCR counts at a rate equivalent to one count per 3.05 μVH, and the DTC counts at a rate of 1.138 counts per second (4096 counts = 1 hour). For example, if no rollover of the DTC register is incipient, a negative 24.42 mV signal produces 8000 DCR counts and 4096 DTC counts each hour. The amount of charge removed from the battery is easily calculated.

During charge, the CCR and the charge time counter (CTC) are active. If $(V_{(SRP)} – V_{(SRN))}$ is greater than 0, indicating a charge, the CCR counts at a rate equivalent to one count per 3.05 μVH, and the CTC counts at a rate of 1.138 counts per seconds. In this case a +24.42-mV signal produces 8000 CCR counts and 4096 CTC counts (assuming no rollover) each hour.

The DTC and the CTC are 16-bit registers, with rollover beyond FFFF hex. If a rollover occurs, the corresponding bit in the MODE register is set, and the counter increments at 1/256 of the normal rate (16 counts per hour.). While in normal operation, the internal RAM and flash registers of the bq26200 may be accessed over the HDQ pin.

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate of 1 count every hour at a nominal 25°C. The SCR count rate doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10°C below 25°C down to 0°C. The value in SCR is useful in estimating the battery self-discharge based on capacity and storage temperature conditions.

Table 4 shows the bq26200 register memory map. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.

Table 1. bq26200 Counters

NAME	DESCRIPTION	RANGE	RAM SIZE
DCR	Discharge count register	$(V_{(SRP)} – V_{(SRN))} < V_{SS}$ (Max. =–100 mV), 3.05 μV/LSB	16-bit
CCR	Charge count register	$(V_{(SRP)} – V_{(SRN))} > Vss$ (Max. = +100 mV), 3.05 μV/LSB	16-bit
SCR	Self-discharge count register	1 count/hour at 25°C	16-bit
DTC	Discharge time counter	1 count/0.8789 s (default), 1 count/225 s if STD is set	16-bit
CTC	Charge time counter	1 count/0.8789 s (default), 1 count/225 s if STC is set	16-bit

APPLICATION INFORMATION

sleep mode operation

The bq26200 begins low-power operation in response to the host issuing the sleep command. Before entering the low-power state, the host processor writes the command to transfer the registers to flash. After the sleep command is sent and the charge/discharge activity is less than the value indicated by the WOE bits shown in Table 3, the chip clock is powered down and data acquisition functions cease except for self-discharge detection. During device sleep the bq26200 periodically wakes briefly to maintain the self-discharge registers. The bq26200 wakes on either a low-to-high or high-to-low transition on the HDQ pin.

Table 2. Operational States

MODE	ACTIVE REGISTERS
Normal	CCR, DCR, CTC, DTC, SDR
Sleep	SDR

Table 3. WOE Thresholds

$WOE_{3–1}$ (HEX)	V_{WOE} (mV)
0h	n/a
1h	3.516
2h	1.758
3h	1.172
4h	0.879
5h	0.703
6h	0.586
7h*	0.502

current sense offset calibration and compensation

The bq26200 automatically and continuously compensates for $V_{(SRP)} – V_{(SRN))}$ offset. No host calibration or compensation is required.

gas gauge control registers

The host maintains the charge and discharge and the self-discharge count registers (CCR, CTC, DCR, DTC, and SCR). To facilitate this maintenance, the bq26200 CLR register resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq26200 completes the reset, the corresponding bit in the CLR register is automatically reset to 0. Clearing the DTC or CTC registers clears the MODE register bits STC/STD and sets the CTC/DTC count rates to the default value of 1.138 counts per second.

device temperature measurement

The bq26200 reports die temperature in units of ºK through register pair TMPH-TMPL. Refer to the TMP register description for more details.

APPLICATION INFORMATION

register interface

Information is exchanged between host system and the bq26200 through the data-register interface. See Table 4 below. The register set consists of a 122-location address space of 8-bit bytes segmented into:

- 8 bytes of factory-programmed ID ROM
- 32 bytes of flash-shadowed RAM
- 64 bytes of general-purpose Flash
- 18 special function registers

Table 4. bq26200 Memory Map

HDQ ADDRESS	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x78–0x7F	IDROM	8 bytes of factory programmed ROM							
0x77	–	Reserved							
0x76	–	Reserved							
0x75	–	Reserved							
0x74	–	Reserved							
0x73	–	Reserved							
0x72	–	Reserved							
0x71		Reserved							
0x70	FPA	Flash program address byte							
0x6F	FPD	Flash program data byte							
0x6E	DCRH	Discharge count register high byte							
0x6D	DCRL	Discharge count register low byte							
0x6C	CCRH	Charge count register high byte							
0x6B	CCRL	Charge count register low byte							
0x6A	SCRH	Self discharge count register high byte							
0x69	SCRL	Self-discharge count register low byte							
0x68	DTCH	Discharge timer counter register high byte							
0x67	DTCL	Discharge timer count register low byte							
0x66	CTCH	Charge timer counter register high byte							
0x65	CTCL	Charge timer counter register low byte							
0x64	MODE/ WOE	RSVD	DISREG	STC	STD	WOE2	WOE1	WOE0	0
0x63	CLR	RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR
0x62	FCMD	Flash/control command register							
0x61	TEMPH	Temperature high byte							
0x60	TEMPL	Temperature low byte							
0x40–0x5F	flash	Page 2, 32 bytes of flash							
0x20–0x3F	flash	Page 1, 32 bytes of flash							
0x00–0x1F	RAM/flash	Page 0, 32 bytes of flash shadowed RAM							

APPLICATION INFORMATION

memory

ID ROM

The bq26200 has 8 bytes of ID ROM. This data field is factory programmed with a unique serial number. Please contact your Texas Instruments representative for details.

flash-shadowed RAM

The host system has direct access to read and modify 32 bytes of RAM. These 32 bytes are shadowed by 32 bytes of flash to provide non-volatile storage of battery conditions. The information stored in RAM is transferred to flash, and the information stored in flash is transferred to RAM by writing a single command into the flash command register (FCMD). When a power-on-reset occurs, PAGE0 of flash is transferred to RAM. For more details, refer to the *flash command register* section.

user-flash memory

In addition to the flash-shadowed RAM, the bq26200 has 64 bytes of user-flash. The user-flash can store specific battery pack parameters, such as charge per VFC pulse, battery chemistry, and self-discharge rates.

flash programming

The two banks of direct user-flash are programmed one byte at a time, but the single bank of flash-shadowed RAM can be programmed one page at a time or by writing the RAM-to-flash transfer code into the flash command register (FCMD). This programming is performed by writing the desired code into the flash command register, FCMD (address 0x62), the host may transfer data between flash and RAM, page erase the flash, place the device into the low power mode, or perform VFC offset measurement. For more details, refer to the *flash command register* section. Summaries of the flash command codes are shown in Table 5.

Table 5. Flash Command Code Summary

COMMAND CODE (HEX)	DESCRIPTION
0x0F	Program byte
0x40	Erase page 0 flash
0x41	Erase page 1 flash
0x42	Erase page 2 flash
0x45	Transfer page 0 RAM to page 0 flash
0x48	Transfer page 0 flash to page 0 RAM
0xF6	Power down

single-byte programming

To program an individual byte in flash, the byte of data is first written into the FPD register while the address to be programmed is written into the FPA register. The program byte command, 0x0F, is then written to the FCMD. The result of this sequence is that the contents of the FPD register are logically AND'd with the contents of the flash address pointed to by the FPA register.

RAM-to-flash transfer

The content of the flash that shadows the user RAM is logically AND'd to the RAM contents when the RAM-to-flash transfer command is sent. If new data is to be written over old data, then it is necessary to first erase the flash page that is being updated and restore all necessary data.

APPLICATION INFORMATION

communicating with the bq26200

The bq26200 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, use the interface to access various bq26200 registers. The HDQ pin requires an external pullup or pulldown resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq26200. The command directs the bq26200 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one and is referenced to V_{SS}. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5 Kbits/s. The least-significant bit of a command or data byte is transmitted first. Data input from the bq26200 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART can also communicate with the bq26200.

If a communication time-out occurs (for example, if the host waits longer than $t_{(CYCD)}$ for the bq26200 to respond or if this is the first access command), then a BREAK should be sent by the host. The host may then re-send the command. The bq26200 detects a BREAK when the HDQ pin is driven to a logic-low state for a time $t_{(B)}$ or greater. The HDQ pin then returns to its normal ready-high logic state for a time $t_{(BR)}$.The bq26200 is then ready for a command from the host processor.

The return-to-one data-bit frame consists of three distinct sections:

1. The first section starts the transmission by either the host or the bq26200 taking the HDQ pin to a low state for a period equal to $t_{(HW1)}$ or $t_{(DW1)}$.
2. The next section is the actual data transmission, where the data should be valid by a period equal to $t_{(HW1)}$ or $t_{(DW1)}$, after the negative edge that starts communication. The data should be held for $t_{(HW0)}$ and $t_{(DW0)}$ periods to allow the host or bq26200 to sample the data bit.
3. The final logic-high state should be held until a period equal to $t_{(CYCH)}$ or $t_{(CYCD)}$, to allow time to ensure that the bit transmission ceased properly.

The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq26200 always occurs with the least-significant bit being transmitted first. Figure 4 shows an example of a communication sequence to read the bq26200 DCRH register.

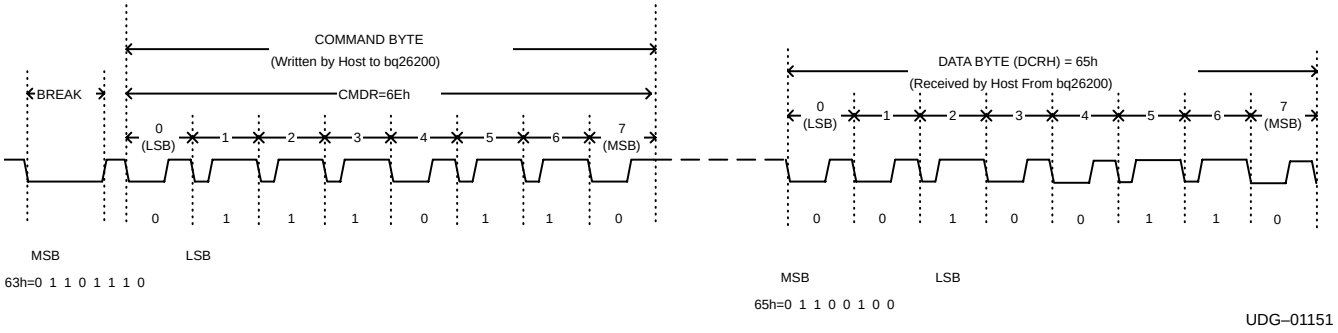


Figure 4. Communication Sequence

APPLICATION INFORMATION

command byte

The command byte of the bq26200 consists of eight contiguous valid command bits. The command byte contains two fields: W/R command and address. The W/R bit of the command register determines whether the command is a read or a write command, while the address field containing bit AD6–AD0 indicates the address to be read or written. The command byte values are shown in table 6.

Table 6. Command Byte

COMMAND BYTE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

W/R W/R indicates whether the command byte is a read or write command. A 1 indicates a write command and that the following eight bits should be written to the register specified by the address field of the command byte, while a 0 indicates that the command is a read. On a read command, the bq26200 outputs the requested register contents specified by the address field portion of the command Byte.

AD6–AD0 AD6–AD0 are the seven bits containing the address portion of the register to be accessed.

bq26200 registers

register maintenance

The host system is responsible for register maintenance. To facilitate this maintenance, the bq26200 clear register (TMP/CLR) resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq26200 completes the reset, the corresponding bit in the TMP/CLR register automatically resets to 0, saving the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of 1 count per 0.8789 s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of 1 count per 0.8789 s.

Table 4 shows the register map for the bq26200.

register descriptions

ID ROM register

The factory programmed 64 bits of ID ROM are located in the eight byte-locations addressed 0x78–0x7f. This data field is factory programmed with a unique serial number. Please contact your Texas Instruments representative for details.

locations 0x71 through 0x77

Locations 0x71 through 0x77 are reserved. Read commands for these registers will return inconsistent results. Write commands will have no affect on these registers.

flash program address register (FPA)

The FPA byte register (address = 0x70) points to the flash address location that will be programmed when the Program flash command is issued. This byte is used with the FPD and FCMD register to program an individual byte in flash memory.

APPLICATION INFORMATION

flash program data register (FPD)

The FPD byte register (address = 0x6F) contains the data to be programmed into the flash address location pointed to by the contents of the FPA register. When the program flash command is issued, the contents of the FPD register are AND'd with the contents of the byte pointed to by the FPA and then stored into that location.

discharge count registers (DCRH/DCRL)

The DCRH high-byte register (address = 0x6E) and the DCRL low-byte register (address =0x6D) contain the count of the discharge, and are incremented whenever $V_{SRP} < V_{SRN}$. These registers continue to count beyond FFFF hex, so proper register maintenance by the host system is necessary. The TMP/CLR register forces the reset of both the DCRH and DCRL to zero.

charge count registers (CCRH/CCRL)

The CCRH high-byte register (address = 0x6C) and the CCRL low-byte register (address = 0x6B) contain the count of the charge, and are incremented whenever $V_{SRP} > V_{SRN}$. These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register forces the reset of both the CCRH and CCRL to zero.

self-discharge count registers (SCRH/SCRL)

The SCRH high-byte register (address = 0x6A) and the SCRL low-byte register (address = 0x69) contain the self-discharge count. This register is continually updated in both the normal operating and sleep modes of the bq26200. The counts in these registers are incremented based on time and temperature. The SCR counts at a rate of 1 count per hour at 20°C to 30°C. The count rate doubles every 10°C up to a maximum of 16 counts/hour at temperatures above 60°C. The count rate halves every 10°C below 20°C to 30°C to a minimum of 1 count/8 hours at temperatures below 0°C. These registers continue to count beyond FFFF hex, so proper register maintenance should be done by the host system. The TMP/CLR register forces the reset of both the SCRH and SCRL to zero. During device sleep the bq26200 periodically wakes for a brief amount of time to maintain the self-discharge registers.

discharge time count registers (DTCH/DTCL)

The DTCH high-byte register (address = 0x68) and the DTCL low-byte register (address = 0x67) determine the length of time the $V_{SRP} < V_{SRN}$ indicating a discharge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the DTCH/DTCL register continues to count beyond FFFF hex, the STD bit is set in the MODE/WOE register, indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

NOTE: Note: If a second rollover occurs, STD is cleared. Access to the bq26200 should be timed to clear DTCH/DTCL more often than every 170 days.

The CLR register forces the reset of both the DTCH and DTCL to zero.

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charge-time count registers (CTCH/CTCL)

The CTCH high-byte register (address = 0x66) and the CTCL low-byte register (address = 0x65) determine the length of time the $V_{SRP} > V_{SRN}$, indicating a charge activity. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond FFFF hex, the STC bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

NOTE: If a second rollover occurs, STC is cleared. Access to the bq26200 should be timed to clear CTCH/CTCL more often than every 170 days. The TMP/CLR register forces the reset of both the CTCH and CTCL to zero.

mode, wake-up enable register (MODE/WOE)

As described below, the MODE/WOE register (address = 0x64) contains regulator disable and the STC and STD bits, and wake-up enable information.

Table 7. MODE/MOE Bits

MODE/WOE BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	DISREG	STC	STD	WOE2	WOE1	WOE0	0

RSVD RSVD bit is reserved for future use and should NOT be modified by the host.

DISREG DISREG is the disable regulator bit, which turns off the internal operational amplifier used in the regulator circuit. In applications where the regulator is not used, the DISREG bit can be set to reduce the bq26200 supply current requirements. A 1 turns off the amplifier while a 0 turns the amplifier on.

STC and STD The slow time charge (STC) and slow time discharge (STD) flags indicate if the CTC or DTC registers have rolled over beyond FFFF hex. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover.

WOE[2..0] The wake-up output enable (WOE) bits (bits 3-1) indicate the voltage level required on the SR pin so that the bq26200 enters sleep mode after a power-down command is issued. Whenever $|V_{SRP} – V_{SRN}| < V_{WOE}$, the bq26200 will enter sleep mode after the power down commands has been issued. On bq26200 power-on reset these bits are set to 1. Setting all of these bits to zero is not valid. Refer to Table 3 for the various WOE values.

BIT0 BIT0 is a reserved bit and must always be set to 0. This bit is cleared on power-on-reset.

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clear register (CLR)

The bits in the CLR register (address 0x63) clear the DCR, CCR, SCR, DTC, and CTC registers indicate if the bq26200 has experienced a power-on-reset and setting the state of the STAT pin as described below:

Table 8. CLR Bits

CLR BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR

RSVD RSVD bit is reserved for future use and should not be modified by the host

POR POR bit indicates a power-on-reset has occurred. This bit is set when V_{CC} has gone below the POR level. This bit can also be set and cleared by the host.

STAT STAT bit, (bit 5), sets the state of the open-drain output of the STAT pin. A 1 turns off the open drain output while a 0 turn the output on. This bit is set to 1 on power-on-reset.

CTC CTC bit, (bit 4), clears the CTCH and CTCL registers and the STC bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the CTC bit is cleared. This bit is cleared on power-on-reset.

DTC DTC bit, (bit 3), clears the DTCH and DTCL registers and the STD bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the DTC bit is cleared. This bit is cleared on power-on-reset.

SCR SCR bit, (bit 2), clears both the SCRH and SCRL registers. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.

CCR CCR bit (bit 1) clears both the CCRH and CCRL registers. Writing a 1 to this bit clears the CCRH and CCRL registers. After these registers are cleared, the CCR bit is cleared. This bit is cleared on power-on-reset.

DCR DCR bit (bit 0) clears both the DCRH and DCRL registers to 0. Writing a 1 to this bit clears the SCRH and SCRL register. Then the SCR bit is cleared. This bit is cleared on power-on-reset.

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flash command register (FCMD)

The FCMD register (address 0x62) is the flash command register. It programs a single flash byte-location, performs flash page erase, transfers RAM to flash and flash to RAM, enters sleep mode. These functions are performed by writing the desired command code to the FCMD register. After the bq26200 has finished executing the issued command, the flash command register is cleared.

0x0F Program byte command code. This code ANDs the contents of the FPD register with the contents of flash byte location pointed to by the contents of the FPA register.

0x40 Erase page 0 command code. This code erases all the bytes of flash from address 0x00 to 0x1F.

0x41 Erase page 1 command code. This code erases all the bytes of flash from address 0x20 to 0x3F.

0x42 Erase page 2 command code. This code erases all the bytes of flash from address 0x40 to 0x5F.

0x45 RAM-to-flash transfer code. This code programs the contents of the RAM into page 0 flash, addresses 0x00 though 0x1F.

0x48 flash to RAM transfer code. This code copies the contents of the page 0 flash into RAM.

0xF6 Power down code. This code places the bq26200 into the sleep mode when the conditions are met as indicated by the WOE bits in the MODE/WOE register. The part remains in sleep mode until a high-to-low or low-to-high transition occurs on the HDQ pin.

temperature registers (TMPH, TMPL)

The TMPH (address 0x61) and the TMPL registers (address 0x60) reports die temperature in hex format in units of °K.

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