



## 18-Bit Analog-to-Digital Converter for Bridge Sensors

### FEATURES

- Complete Front-End for Bridge Sensor
- Internal Amplifier, Gain of 64
- Internal Oscillator
- Low-Side Power Switch for Bridge Sensor
- 18-Bit Noise-Free Resolution
- Selectable 10SPS or 80SPS Data Rates
- Simultaneous 50Hz and 60Hz Rejection at 10SPS
- External Voltage Reference up to 5V for Ratiometric Measurements
- Simple, Pin-Driven Control
- Two-Wire Serial Digital Interface
- Tiny TSSOP-16 Package
- Supply Range: 2.7V to 5.3V
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Temperature Range

### APPLICATIONS

- Weigh Scales
- Strain Gauges
- Load Cells
- Industrial Process Control

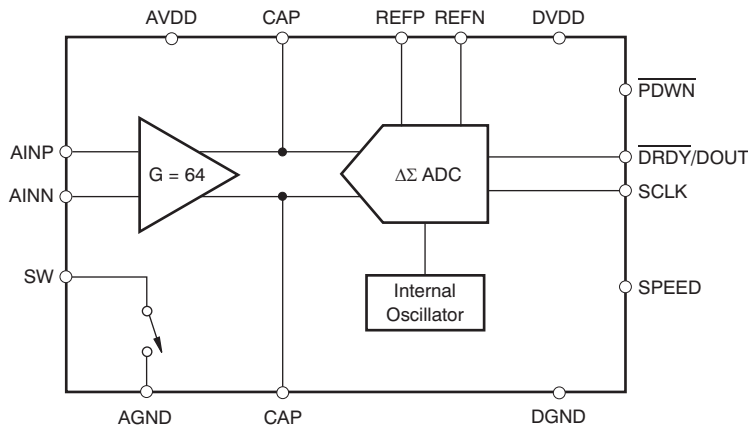
### DESCRIPTION

The ADS1131 is a precision, 18-bit analog-to-digital converter (ADC). With an onboard, low-noise amplifier, onboard oscillator, precision 18-bit delta-sigma ( $\Delta\Sigma$ ) ADC, and bridge power switch, the ADS1131 provides a complete front-end solution for bridge sensor applications including weigh scales, strain gauges, and load cells.

The low-noise amplifier has a gain of 64, supporting a full-scale differential input of  $\pm 39\text{mV}$ . The  $\Delta\Sigma$  ADC has 18-bit effective resolution and is comprised of a third-order modulator and fourth-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1131 can be put in a low-power standby mode or shut off completely in power-down mode.

All of the features of the ADS1131 are controlled by dedicated pins; there are no digital registers to program. Data are output over an easily-isolated serial interface that connects directly to the MSP430 and other microcontrollers.

The ADS1131 is available in a TSSOP-16 package and is specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . The [ADS1231](#) offers a 24-bit upgrade to the ADS1131.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

	ADS1131	UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +6	V
AGND to DGND	–0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog input voltage to AGND	–0.3 to AVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +85	°C
Storage temperature range	–60 to +150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

Minimum/maximum limit specifications apply from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Typical specifications at  $+25^{\circ}\text{C}$ .  
All specifications at  $\text{AVDD} = \text{DVDD} = \text{REFP} = +5\text{V}$ , and  $\text{REFN} = \text{AGND}$ , unless otherwise noted.

PARAMETER	CONDITIONS	ADS1131			UNIT
		MIN	TYP	MAX	
<b>ANALOG INPUTS</b>					
Full-scale input voltage ( $\text{AINP} - \text{AINN}$ )		$\pm 0.5V_{\text{REF}}/64$			V
	$V_{\text{REF}} = \text{AVDD} = 5\text{V}$	$\pm 39.0$			mV
	$V_{\text{REF}} = \text{AVDD} = 3\text{V}$	$\pm 23.4$			mV
Common-mode input range		AGND + 1.5V		AVDD – 1.5V	V
Differential input current			$\pm 2$		nA
<b>LOW-SIDE POWER SWITCH</b>					
On-resistance ( $R_{\text{ON}}$ )	AVDD = 5V		TBD		$\Omega$
	AVDD = 3V		TBD		$\Omega$
Current-through switch				30	mA
<b>SYSTEM PERFORMANCE</b>					
Resolution	No missing codes	18			Bits
Data rate	SPEED = high	80			SPS
	SPEED = low	10			SPS
Digital filter settling time	Full settling	4			Conversions
Integral nonlinearity (INL)	Differential input, end-point fit	$\pm 10$			ppm
Input offset error <sup>(1)</sup>		TBD			ppm of FS
Input offset drift		$\pm 10$			nV/ $^{\circ}\text{C}$
Gain error		$\pm 0.8$			%
Gain drift		$\pm 4$			ppm/ $^{\circ}\text{C}$
Normal-mode rejection <sup>(2)</sup>	$f_{\text{IN}} = 50\text{Hz}$ or $60\text{Hz} \pm 1\text{Hz}$ , $f_{\text{DATA}} = 10\text{SPS}$	90			dB
Common-mode rejection	At dc	110			dB
Input-referred noise	$f_{\text{DATA}} = 10\text{SPS}$ , AVDD = $V_{\text{REF}} = 5\text{V}$	1			LSB
	$f_{\text{DATA}} = 80\text{SPS}$ , AVDD = $V_{\text{REF}} = 5\text{V}$	1.7			LSB
	AVDD = 5V	$\pm 39.0$			mV
	AVDD = 3V	$\pm 23.4$			mV
Power-supply rejection	At dc	90	100		dB
<b>VOLTAGE REFERENCE INPUT</b>					
Voltage reference input ( $V_{\text{REF}}$ )	$V_{\text{REF}} = \text{REFP} - \text{REFN}$	1.5	AVDD	AVDD + 0.1V	V
Negative reference input (REFN)		AGND – 0.1		REFP – 1.5	V
Positive reference input (REFP)		REFN + 1.5		AVDD + 0.1	V
Voltage reference input current			10		nA
<b>DIGITAL</b>					
Logic levels	$V_{\text{IH}}$	All digital inputs except CLKIN	0.7 DVDD	DVDD + 0.1	V
		CLKIN	0.7 DVDD	5.1	V
	$V_{\text{IL}}$		DGND	0.2 DVDD	V
	$V_{\text{OH}}$	$I_{\text{OH}} = 1\text{mA}$	DVDD – 0.4		V
	$V_{\text{OL}}$	$I_{\text{OL}} = 1\text{mA}$		0.2 DVDD	V
Input leakage	$0 < V_{\text{IN}} < \text{DVDD}$			$\pm 10$	$\mu\text{A}$
Serial clock input frequency ( $f_{\text{SCLK}}$ )				5	MHz

(1) Offset calibration can minimize these errors to the level of noise at any temperature.

(2) Specification is assured by the combination of design and final production test.

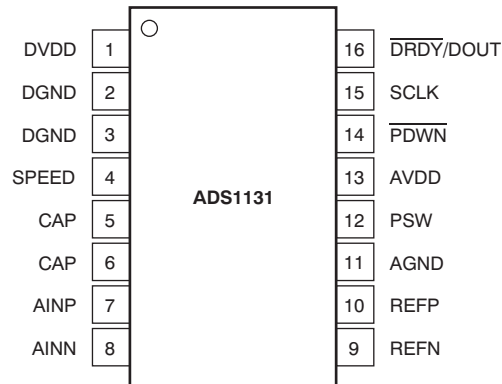
**ELECTRICAL CHARACTERISTICS (continued)**

Minimum/maximum limit specifications apply from –40°C to +85°C. Typical specifications at +25°C.  
All specifications at AVDD = DVDD = REFP = +5V, and REFN = AGND, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1131			UNIT
		MIN	TYP	MAX	
<b>POWER SUPPLY</b>					
Power-supply voltage (AVDD, DVDD)		2.7		5.3	V
Analog supply current	Normal mode, AVDD = 3V		900	1400	μA
	Normal mode, AVDD = 5V		900	1400	μA
	Standby mode		0.1		μA
	Power-down		0.1		μA
Digital supply current	Normal mode, DVDD = 3V		60	100	μA
	Normal mode, DVDD = 5V		95	140	μA
	Standby mode, SCLK = high, DVDD = 3V		45	65	μA
	Standby mode, SCLK = high, DVDD = 5V		65	80	μA
	Power-down		0.2		μA
Power dissipation, total	Normal mode, AVDD = DVDD = 3V		2.9	4.5	mW
	Normal mode, AVDD = DVDD = 5V		5.0	7.7	mW
	Standby mode, AVDD = DVDD = 5V		0.3		mW
<b>TEMPERATURE</b>					
Operating temperature range		–40		+85	°C
Specified temperature range		–40		+85	°C

## PIN CONFIGURATION

**PW PACKAGE  
TSSOP-16  
(Top View)**



## PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION	
DVDD	1	Digital	Digital power supply: 2.7V to 5.3V	
DGND	2, 3	Digital	Digital ground	
SPEED	4	Digital input	Data rate select:	
			<b>SPEED</b>	<b>DATA RATE</b>
			0	10SPS
			1	80SPS
CAP	5	Analog	Gain amplifier bypass capacitor connection	
CAP	6	Analog	Gain amplifier bypass capacitor connection	
AINP	7	Analog input	Positive analog input	
AINN	8	Analog input	Negative analog input	
REFN	9	Analog input	Negative reference input	
REFP	10	Analog input	Positive reference input	
AGND	11	Analog	Analog ground	
AVDD	13	Analog	Analog power supply, 2.7V to 5.3V	
PSW	12	Analog	Low-side power switch	
PDWN	14	Digital input	Power-down: holding this pin low powers down the entire converter and resets the ADC.	
SCLK	15	Digital input	Serial clock: clock out data on the rising edge. Also used to initiate Offset Calibration and Sleep modes. See the <a href="#">Standby Mode</a> section for more details.	
DRDY/DOUT	16	Digital output	Dual-purpose output: Data ready: indicates valid data by going low. Data output: outputs data, MSB first, on the first rising edge of SCLK.	

**PRODUCT PREVIEW**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ADS1131ID	PREVIEW	SOIC	D	16	40	TBD	Call TI	Call TI
ADS1131IDR	PREVIEW	SOIC	D	16	2500	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

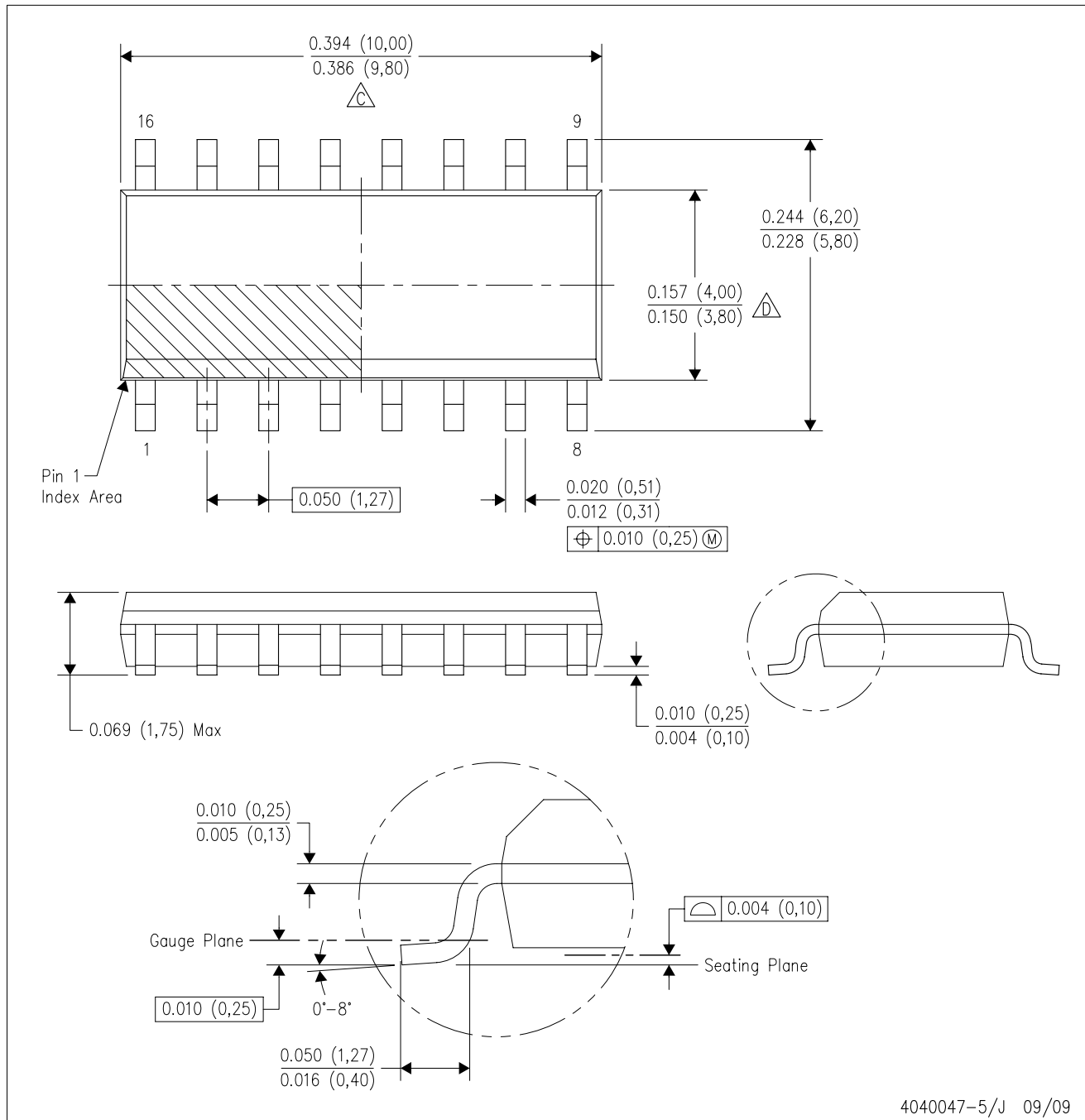
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
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