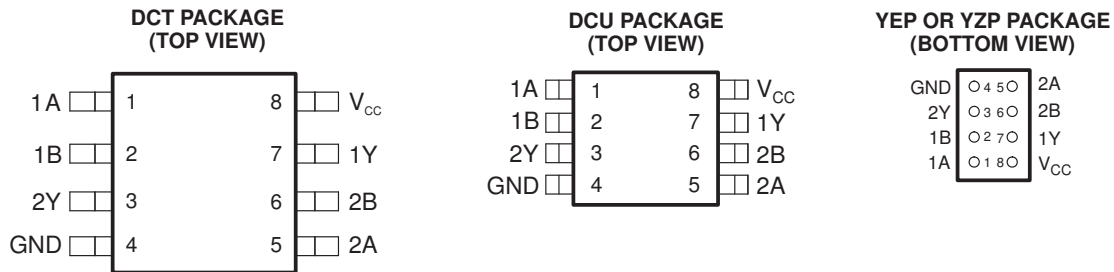


FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.7 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual 2-input exclusive-OR gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC2G86 performs the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AUC2G86YEPR	PREVIEW
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUC2G86YZPR	
	SSOP – DCT	Tape and reel	SN74AUC2G86DCTR	U86_ _ _
	VSSOP – DCU	Tape and reel	SN74AUC2G86DCUR	U86_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



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SN74AUC2G86 DUAL 2-INPUT EXCLUSIVE-OR GATE

SCES479A – AUGUST 2003 – REVISED JUNE 2006

DESCRIPTION/ORDERING INFORMATION

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

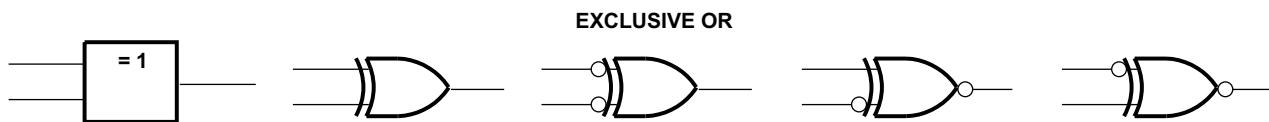
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLE
(each gate)**

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

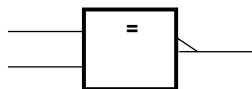
EXCLUSIVE-OR LOGIC

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



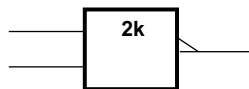
These are five equivalent exclusive-OR symbols valid for an SN74AUC2G86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



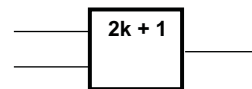
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	3.6	V
V _I	Input voltage range ⁽²⁾	-0.5	3.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	3.6	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±20 mA
Continuous current through V _{CC} or GND				±100 mA
θ _{JA}	Package thermal impedance ⁽³⁾	DCT package		220 °C/W
		DCU package		227
		YEP/YZP package		102
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.7	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	-0.7	mA
		V _{CC} = 1.1 V	-3	
		V _{CC} = 1.4 V	-5	
		V _{CC} = 1.65 V	-8	
		V _{CC} = 2.3 V	-9	
I _{OL}	Low-level output current	V _{CC} = 0.8 V	0.7	mA
		V _{CC} = 1.1 V	3	
		V _{CC} = 1.4 V	5	
		V _{CC} = 1.65 V	8	
		V _{CC} = 2.3 V	9	
Δt/Δv	Input transition rise or fall rate			20 ns/V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AUC2G86

DUAL 2-INPUT EXCLUSIVE-OR GATE

SCES479A–AUGUST 2003–REVISED JUNE 2006

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} - 0.1			V
		I _{OH} = -0.7 mA	0.8 V	0.55			
		I _{OH} = -3 mA	1.1 V	0.8			
		I _{OH} = -5 mA	1.4 V	1			
		I _{OH} = -8 mA	1.65 V	1.2			
		I _{OH} = -9 mA	2.3 V	1.8			
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V			0.2	V
		I _{OL} = 0.7 mA	0.8 V	0.25			
		I _{OL} = 3 mA	1.1 V			0.3	
		I _{OL} = 5 mA	1.4 V			0.4	
		I _{OL} = 8 mA	1.65 V			0.45	
		I _{OL} = 9 mA	2.3 V			0.6	
I _I	A or B inputs	V _I = V _{CC} or GND	0 to 2.7 V			±5	μA
I _{off}		V _I or V _O = 2.7 V	0			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V			10	μA
C _i		V _I = V _{CC} or GND	2.5 V		2.5		pF

(1) All typical values are at T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	5.3	0.8	3.8	0.5	2.6	0.4	1	1.7	0.3	1.3	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8	1.5	2.6	0.7	2	ns

Operating Characteristics

T_A = 25°C

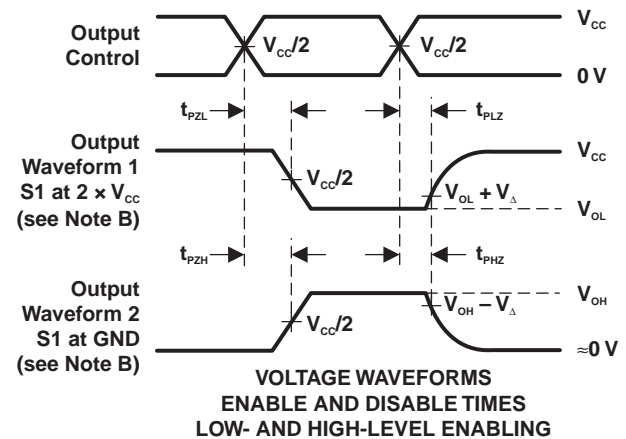
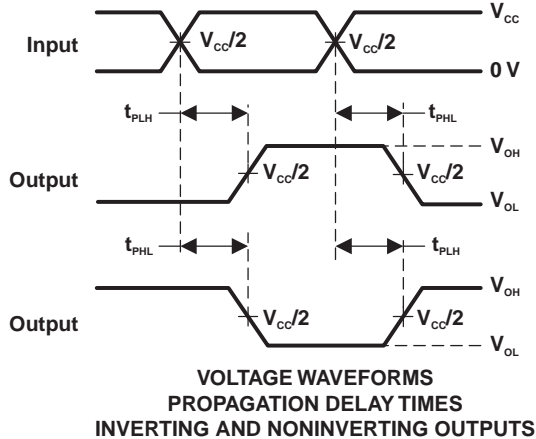
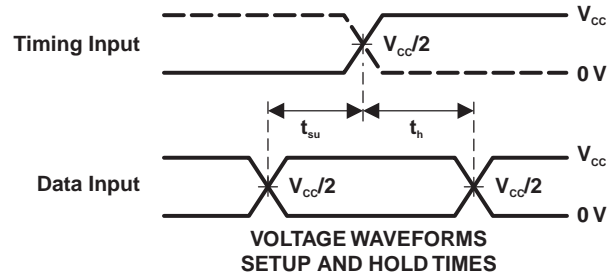
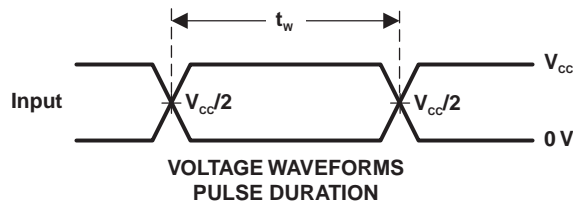
PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
		TYP	TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance f = 10 MHz	15	15	16	19	27	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
1.8 V \pm 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	30 pF	500 Ω	0.15 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate \geq 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PZL} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUC2G86DCTR	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G86DCTRE4	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G86DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G86DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G86YEPR	NRND	WCSP	YEP	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74AUC2G86YZPR	ACTIVE	WCSP	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

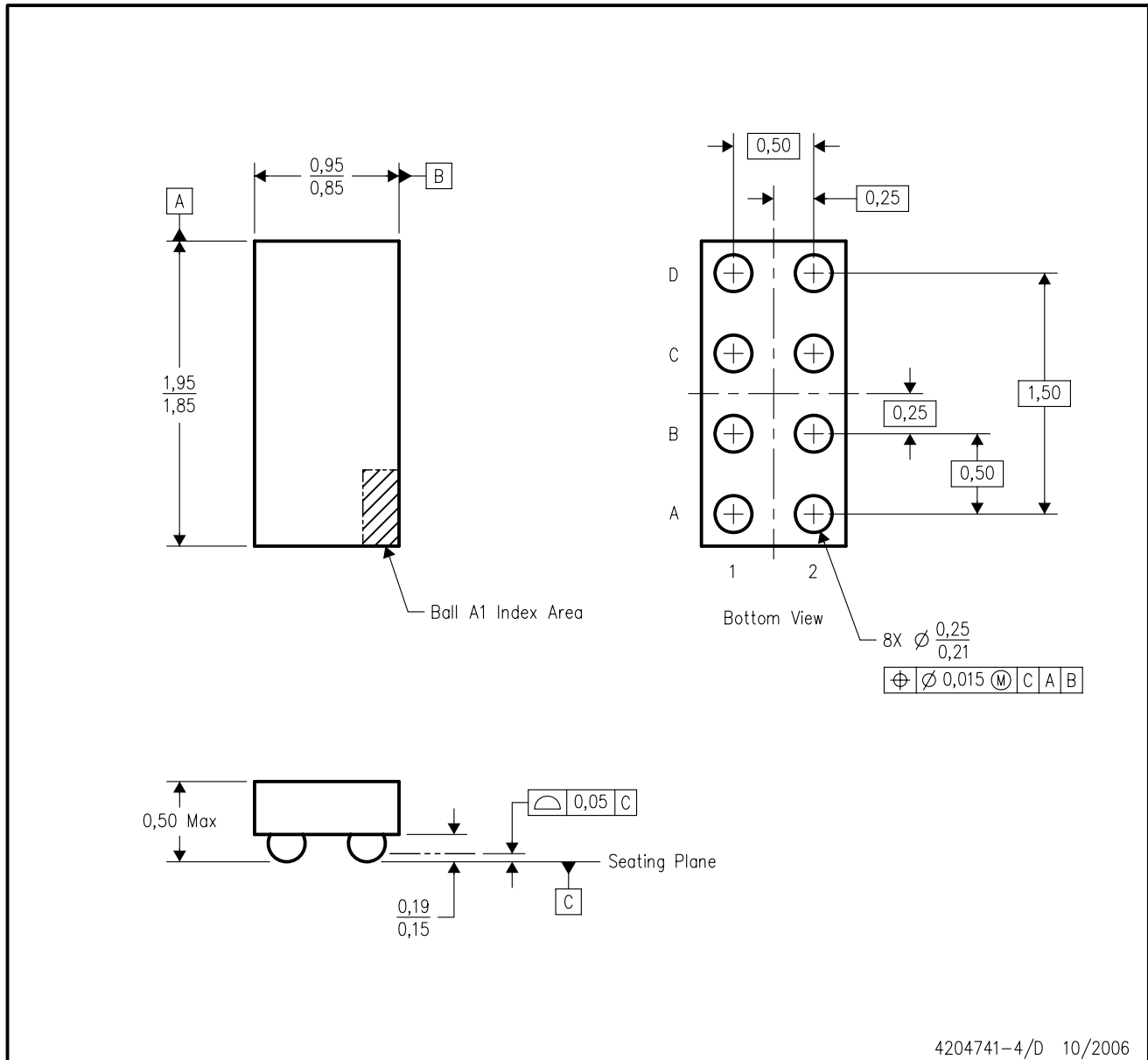
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY

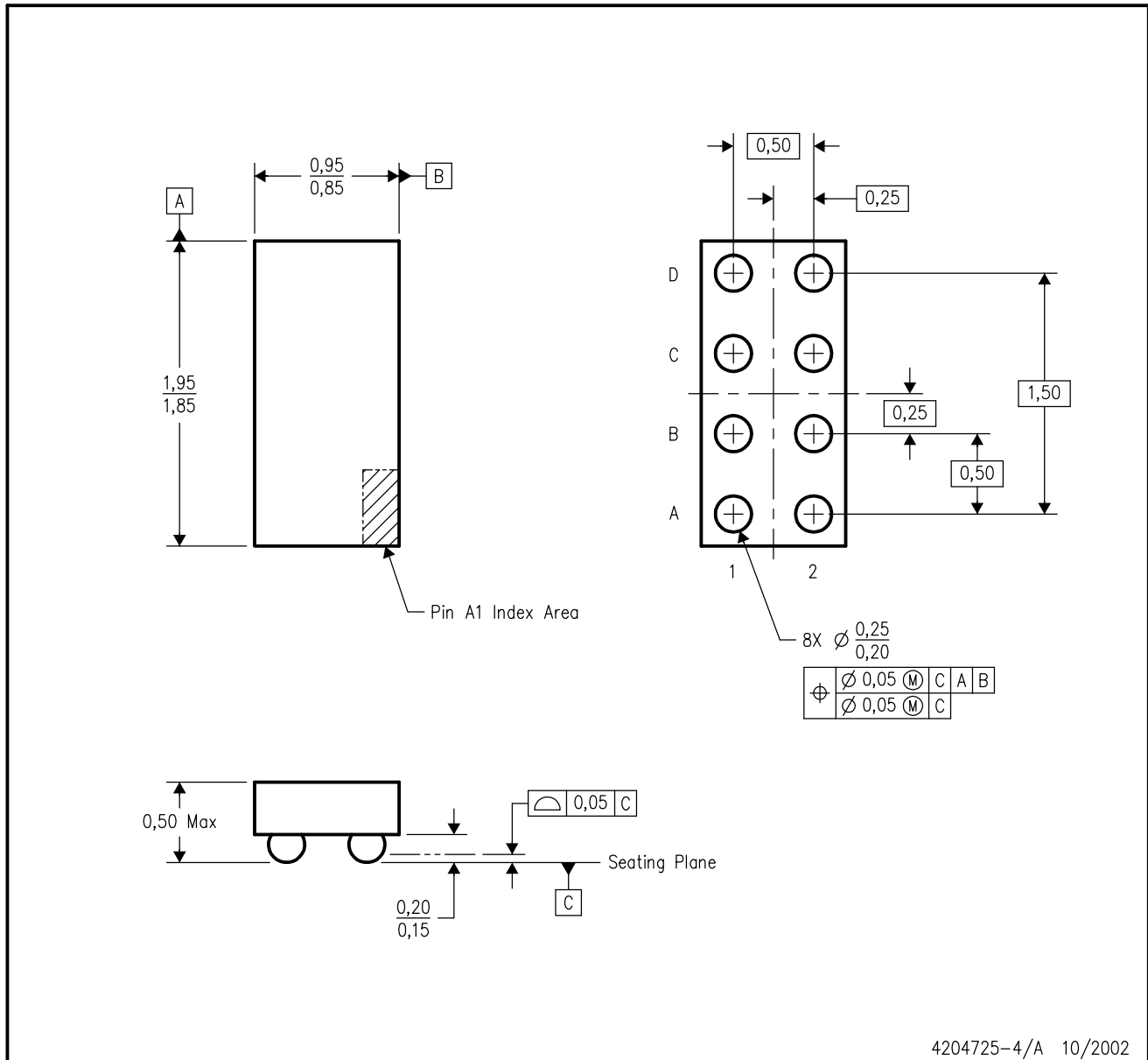


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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