# **Power MOSFET**

# 80 V, 25.5 m $\Omega$ , 25 A, Dual N-Channel

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- NVMFD6H852NLWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	80	٧
Gate-to-Source Voltage	Э		V <sub>GS</sub>	±20	٧
Continuous Drain	Steady	T <sub>C</sub> = 25°C	I <sub>D</sub>	25	Α
Current R <sub>θJC</sub> (Notes 1, 2, 3)		T <sub>C</sub> = 100°C		18	
Power Dissipation	State	T <sub>C</sub> = 25°C	$P_{D}$	38	W
R <sub>θJC</sub> (Notes 1, 2)		T <sub>C</sub> = 100°C	1	19	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	7	Α
Current R <sub>θJA</sub> (Notes 1, 2, 3)	Steady	T <sub>A</sub> = 100°C	1	5	
Power Dissipation	State	T <sub>A</sub> = 25°C	$P_{D}$	3.2	W
R <sub>θJA</sub> (Notes 1, 2)		T <sub>A</sub> = 100°C	1	1.6	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I <sub>DM</sub>	98	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			Is	32	Α
Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, I <sub>L(pk)</sub> = 1.3 A)			E <sub>AS</sub>	86	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	3.95	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	47.3	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

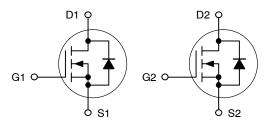


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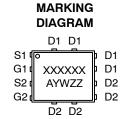
#### www.onsemi.com

V <sub>(BR)DS</sub>	; 1	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
80 V	25	5.5 mΩ @ 10 V	05 A
80 V	31	.5 mΩ @ 4.5 V	25 A

#### **Dual N-Channel**







A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

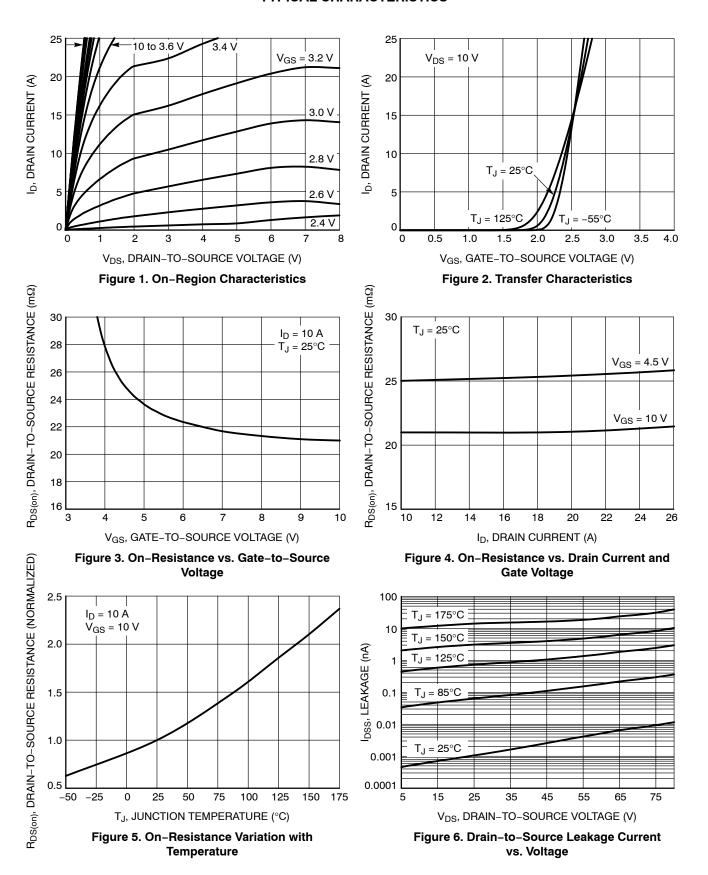
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				47.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	T <sub>J</sub> = 25 °C			10	
		V <sub>DS</sub> = 80 V	T <sub>J</sub> = 125°C			250	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{G}$	<sub>S</sub> = 20 V			100	nA
ON CHARACTERISTICS (Note 4)					-		
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 26 \mu A$		1.2		2.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A		21	25.5	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 10 A		25	31.5	
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 10 A			138		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE			•		•	-
Input Capacitance	C <sub>ISS</sub>	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz, V}_{DS} = 40 \text{ V}$ $V_{GS} = 10 \text{ V, V}_{DS} = 40 \text{ V; I}_{D} = 10 \text{ A}$			521		
Output Capacitance	Coss				69		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				4		
Total Gate Charge	Q <sub>G(TOT)</sub>				10		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 40 V; I <sub>D</sub> = 10 A			5		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				1.1		
Gate-to-Source Charge	Q <sub>GS</sub>				1.9		
Gate-to-Drain Charge	$Q_{GD}$				1.7		
Plateau Voltage	$V_{GP}$				3.1		V
SWITCHING CHARACTERISTICS (Note	5)			•	•	•	
Turn-On Delay Time	t <sub>d(ON)</sub>				7		
Rise Time	t <sub>r</sub>	VGS = 4.5 V. Vr	ne = 64 V.		23		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 64 \text{ V},$ $I_{D} = 10 \text{ A}, R_{G} = 2.5 \Omega$			19		ns ns
Fall Time	t <sub>f</sub>				16		
DRAIN-SOURCE DIODE CHARACTERIS	STICS			1		1	
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A	T <sub>J</sub> = 25°C		0.8	1.2	
			T <sub>J</sub> = 125°C		0.7		_ v
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 10 \text{ A}$			25		
Charge Time	ta				18		ns
Discharge Time	t <sub>b</sub>				7		
Reverse Recovery Charge	Q <sub>RR</sub>				20		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



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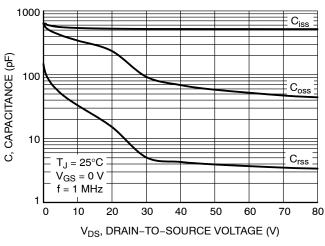


Figure 7. Capacitance Variation

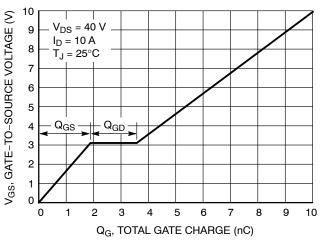


Figure 8. Gate-to-Source vs. Total Charge

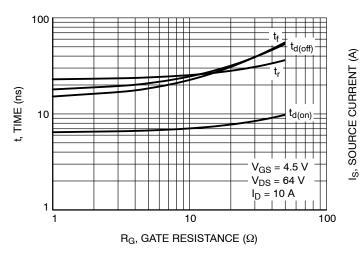


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

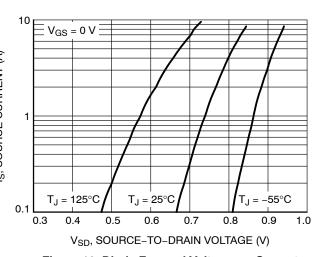


Figure 10. Diode Forward Voltage vs. Current

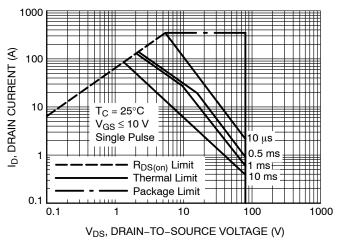


Figure 11. Maximum Rated Forward Biased Safe Operating Area

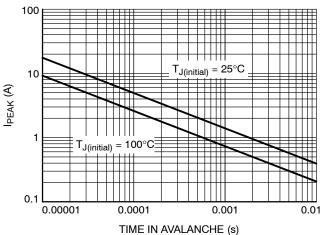


Figure 12. Maximum Drain Current vs. Time in Avalanche

## **TYPICAL CHARACTERISTICS**

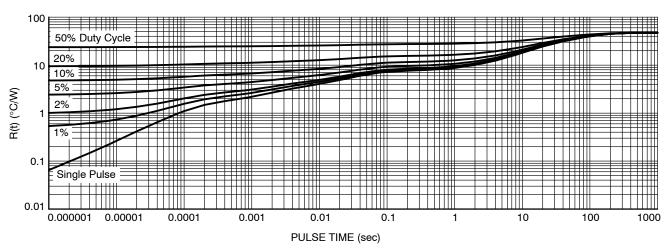


Figure 13. Thermal Response

## **DEVICE ORDERING INFORMATION**

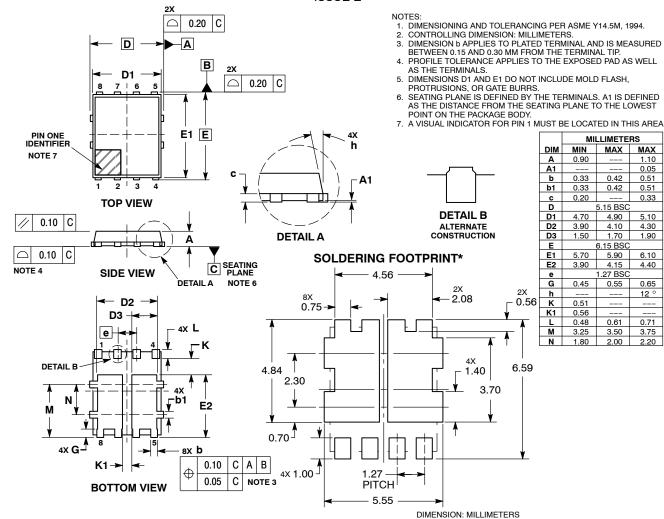
Device	Marking	Package	Shipping <sup>†</sup>
NVMFD6H852NLT1G	6H852L	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD6H852NLWFT1G	852LWF	DFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

# DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT **ISSUE E** 



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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