74AHC125; 74AHCT125

Quad buffer/line driver; 3-state

Rev. 03 — 24 March 2006 Product data sheet

1. General description

The 74AHC125; 74AHCT125 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74AHC125; 74AHCT125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The 74AHC125; 74AHCT125 is identical to the 74AHC126; 74AHCT126 but has active LOW enable inputs.

2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For 74AHC125 only: operates with CMOS input levels
- For 74AHCT125 only: operates with TTL input levels
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-C exceeds 200 V
  - CDM EIA/JESD22-C101-C exceeds 1000 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Quick reference data

Table 1. Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = ≤ 3.0 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74AHC125							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 5 V; C_L = 15 pF		-	3.0	5.5	ns
C_i	input capacitance	$V_I = V_{CC}$ or GND		-	3.0	10	pF
C_o	output capacitance			-	4.0	-	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[1]	-	10	-	pF

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Table 1. Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = ≤ 3.0 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74AHCT125							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 5 V; C_L = 15 pF		-	3.0	3.5	ns
C_i	input capacitance	$V_I = V_{CC}$ or GND		-	3.0	10	pF
C_o	output capacitance			-	4.0	-	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[1]	-	12	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC125				
74AHC125D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC125PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT125				
74AHCT125D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT125PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

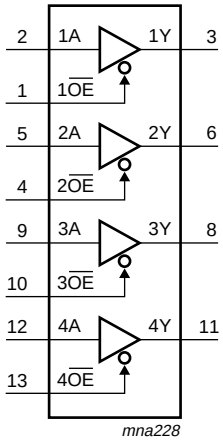


Fig 1. Functional diagram

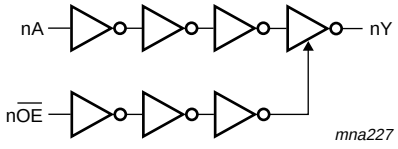


Fig 2. Logic diagram

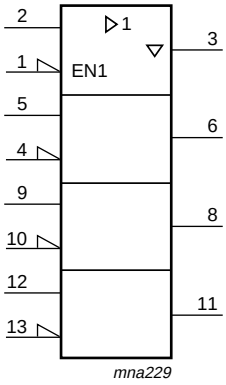


Fig 3. IEC logic diagram

6. Pinning information

6.1 Pinning

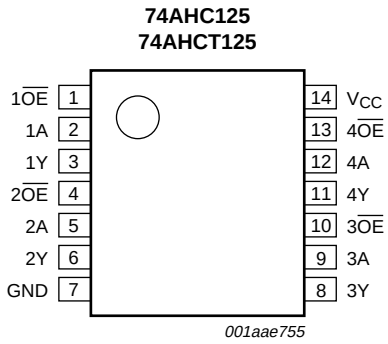


Fig 4. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input 1OE_N (active LOW)
1A	2	data input 1A
1Y	3	data output 1Y
$2\overline{OE}$	4	output enable input 2OE_N (active LOW)
2A	5	data input 2A
2Y	6	data output 2Y
GND	7	ground (0 V)
3Y	8	data output 3Y
3A	9	data input 3A
$3\overline{OE}$	10	output enable input 3OE_N (active LOW)
4Y	11	data output 4Y
4A	12	data input 4A
$4\overline{OE}$	13	output enable input 4OE_N (active LOW)
V_{CC}	14	supply voltage

7. Functional description

7.1 Function table

Table 4. Function table[1]

Control	Input	Output
$n\overline{OE}$	nA	nY
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	-	–20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	V_O = –0.5 V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	quiescent supply current			-	75	mA
I_{GND}	ground current			-	–75	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
	SO14 package		[2]	-	500	mW
	TSSOP14 package		[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC125						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	ns/V
		V_{CC} = 5 V ± 0.5 V	-	-	20	ns/V
74AHCT125						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 5 V ± 0.5 V	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics 74AHC125

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	3.0	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.36	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.1	µA

Table 7. Static characteristics 74AHC125 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.25	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	µA
C_i	input capacitance		-	3.0	10	pF
C_o	output capacitance		-	4.0	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −50 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −50 µA; V_{CC} = 3.0 V	2.9	-	-	V
		I_O = −50 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.48	-	-	V
		I_O = −8.0 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.44	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±2.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20	µA
C_i	input capacitance		-	-	10	pF

Table 7. Static characteristics 74AHC125 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	-	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.40	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.70	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	2.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	µA
C_i	input capacitance		-	-	10	pF

Table 8. Static characteristics 74AHCT125

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.36	V
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V	-	-	0.1	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND per input pin; other pins at V_{CC} or GND; I_O = 0 A	-	-	±0.25	µA

Table 8. Static characteristics 74AHCT125 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other pins at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.35	mA
C_i	input capacitance		-	3.0	10	pF
C_o	output capacitance		-	4.0	-	pF
$T_{amb} = -40$ °C to +85 °C						
V_{IH}	HIGH-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.8	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.44	V
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V	-	-	1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other pins at V_{CC} or GND; $I_O = 0$ A	-	-	±2.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	20	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other pins at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA
C_i	input capacitance		-	-	10	pF
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.70	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.55	V
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V	-	-	2.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other pins at V_{CC} or GND; $I_O = 0$ A	-	-	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other pins at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA
C_i	input capacitance		-	-	10	pF

11. Dynamic characteristics

Table 9. Dynamic characteristics 74AHC125

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C [1]							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 5					
		C_L = 15 pF		-	4.4	8.0	ns
		C_L = 50 pF		-	6.2	11.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 5					
		C_L = 15 pF		-	3.0	5.5	ns
		C_L = 50 pF			4.3	7.5	ns
t_{PZL}, t_{PZH}	output enable time n$\overline{OE}$ to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 6					
		C_L = 15 pF		-	4.7	8.0	ns
		C_L = 50 pF		-	6.8	11.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		-	3.3	5.1	ns
		C_L = 50 pF		-	4.7	7.1	ns
t_{PLZ}, t_{PHZ}	output disable time n$\overline{OE}$ to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 6					
		C_L = 15 pF		-	6.7	9.7	ns
		C_L = 50 pF		-	9.6	13.2	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		-	4.8	6.8	ns
		C_L = 50 pF		-	6.8	8.8	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[2]	-	10	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 5					
		C_L = 15 pF		1.0	-	9.5	ns
		C_L = 50 pF		1.0	-	13.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 5					
		C_L = 15 pF		1.0	-	6.5	ns
		C_L = 50 pF		1.0	-	8.5	ns
t_{PZL}, t_{PZH}	output enable time n$\overline{OE}$ to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 6					
		C_L = 15 pF		1.0	-	9.5	ns
		C_L = 50 pF		1.0	-	13.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		1.0	-	6.0	ns
		C_L = 50 pF		1.0	-	8.0	ns

Table 9. Dynamic characteristics 74AHC125 *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLZ}, t_{PHZ}	output disable time $n\overline{OE}$ to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 6				
		C_L = 15 pF	1.0	-	11.5	ns
		C_L = 50 pF	1.0	-	15.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 6				
		C_L = 15 pF	1.0	-	8.0	ns
		C_L = 50 pF	1.0	-	10.0	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 5				
		C_L = 15 pF	1.0	-	11.5	ns
		C_L = 50 pF	1.0	-	14.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 5				
		C_L = 15 pF	1.0	-	7.0	ns
		C_L = 50 pF	1.0	-	9.5	ns
t_{PZL}, t_{PZH}	output enable time $n\overline{OE}$ to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 6				
		C_L = 15 pF	1.0	-	11.5	ns
		C_L = 50 pF	1.0	-	14.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 6				
		C_L = 15 pF	1.0	-	6.5	ns
		C_L = 50 pF	1.0	-	9.0	ns
t_{PLZ}, t_{PHZ}	output disable time $n\overline{OE}$ to nY	V_{CC} = 3.0 V to 3.6 V; see Figure 6				
		C_L = 15 pF	1.0	-	12.5	ns
		C_L = 50 pF	1.0	-	16.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 6				
		C_L = 15 pF	1.0	-	8.5	ns
		C_L = 50 pF	1.0	-	11.0	ns

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 10. Dynamic characteristics 74AHCT125

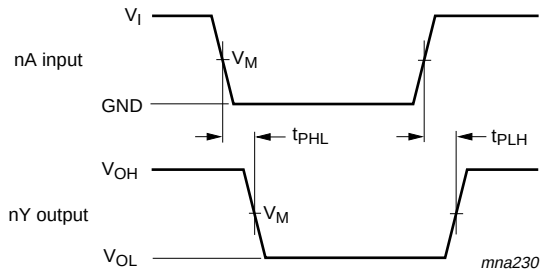
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C [1]							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 5					
		C_L = 15 pF		-	3.0	5.5	ns
		C_L = 50 pF		-	4.3	7.5	ns
t_{PZL}, t_{PZH}	output enable time n$\overline{OE}$ to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		-	3.4	5.1	ns
		C_L = 50 pF		-	4.9	7.3	ns
t_{PLZ}, t_{PHZ}	output disable time n$\overline{OE}$ to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		-	4.5	6.8	ns
		C_L = 50 pF		-	6.5	8.8	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[2]	-	12	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 5					
		C_L = 15 pF		1.0	-	6.5	ns
		C_L = 50 pF		1.0	-	8.5	ns
t_{PZL}, t_{PZH}	output enable time n$\overline{OE}$ to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		1.0	-	6.0	ns
		C_L = 50 pF		1.0	-	8.3	ns
t_{PLZ}, t_{PHZ}	output disable time n$\overline{OE}$ to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		1.0	-	8.0	ns
		C_L = 50 pF		1.0	-	10.0	ns
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 5					
		C_L = 15 pF		1.0	-	7.0	ns
		C_L = 50 pF		1.0	-	9.5	ns
t_{PZL}, t_{PZH}	output enable time n$\overline{OE}$ to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		1.0	-	6.5	ns
		C_L = 50 pF		1.0	-	9.5	ns
t_{PLZ}, t_{PHZ}	output disable time n$\overline{OE}$ to nY	V_{CC} = 4.5 V to 5.5 V; see Figure 6					
		C_L = 15 pF		1.0	-	8.5	ns
		C_L = 50 pF		1.0	-	11.0	ns

[1] Typical values are measured at nominal supply voltage (V_{CC} = 5.0 V).

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

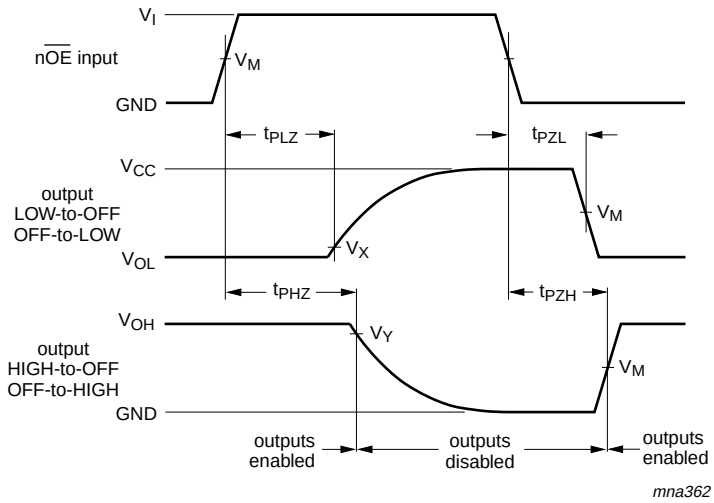
12. Waveforms



Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. Propagation delay input (nA) to output (nY)



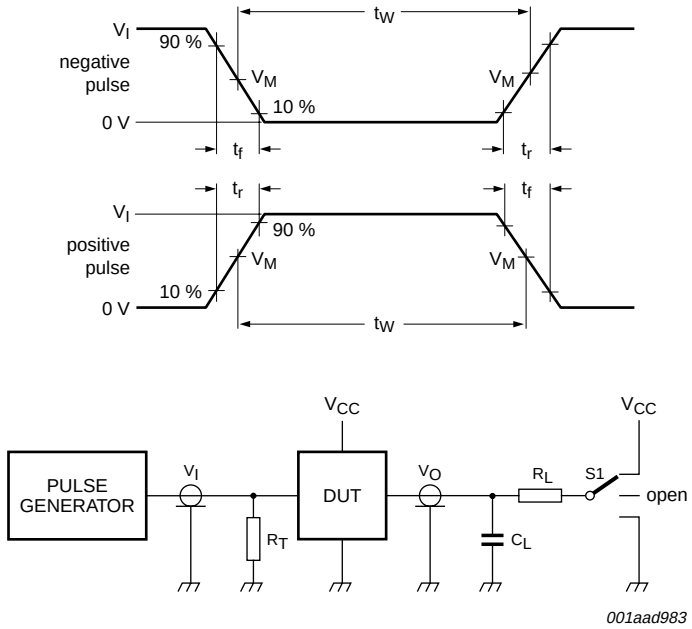
Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. 3-state enable and disable times

Table 11. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC125	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OL} – 0.3 V
74AHCT125	1.5 V	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OL} – 0.3 V



Test data is given in Table 12.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

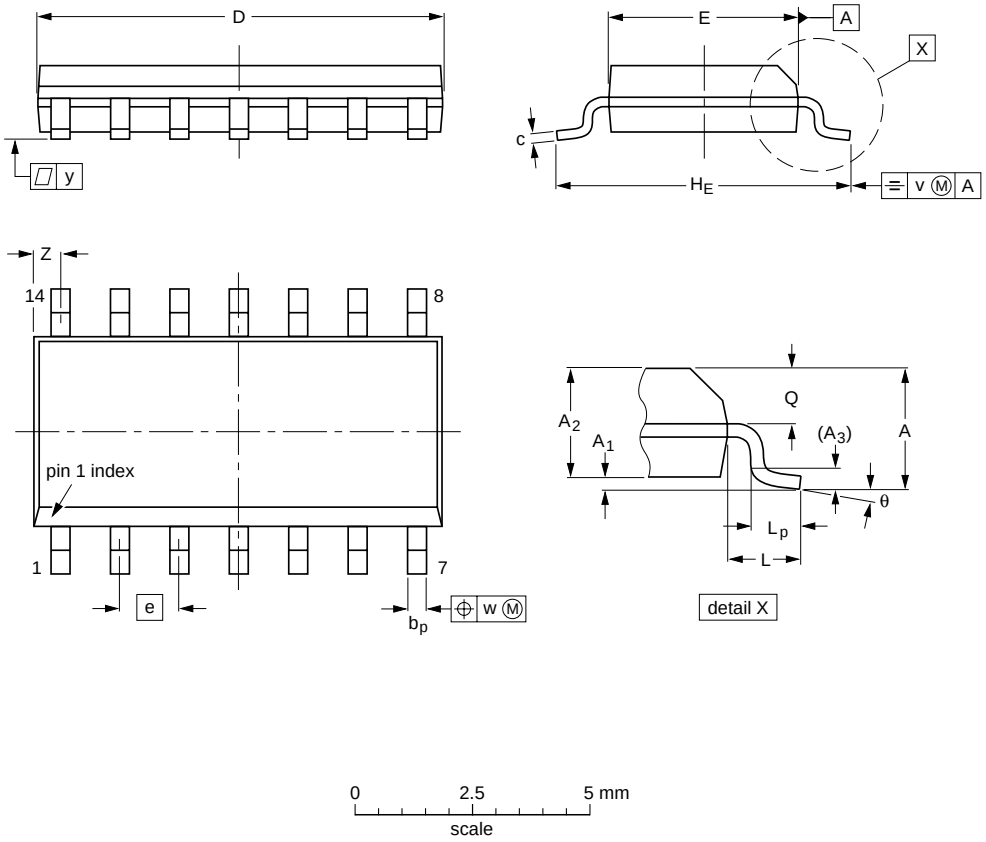
Fig 7. Load circuitry for switching times

Table 12. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC125	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT125	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

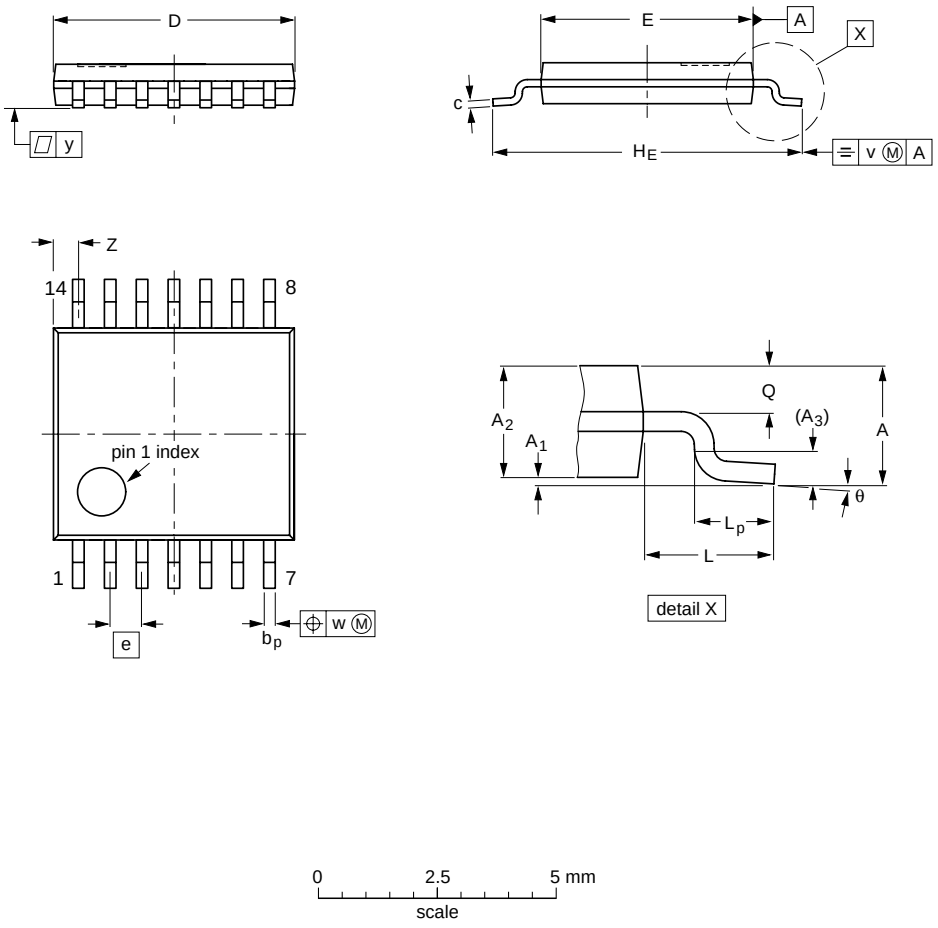
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT125_3	20060324	Product data sheet	-	74AHC_AHCT125_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2: value changed for Machine Model • Table 2: deleted North American type numbers			
74AHC_AHCT125_2	19990927	Product specification	-	74AHC_AHCT125_N_1
74AHC_AHCT125_N_1	19990111	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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