SAM D5x/E5x Family Silicon Errata and Data Sheet Clarification

SAM D5x/E5x Family Errata

The SAM D5x/E5x family of devices that you have received conform functionally to the current preliminary Device Data Sheet (DS60001507**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. SAM D5x/E5x Family Silicon Device Identification. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the SAM D5x/E5x family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. SAM D5x/E5x Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])	
		A	D
ATSAME54P19A	0x61840x01	0x0	0x3
ATSAME54P20A	0x61840x00		
ATSAME54N19A	0x61840x03		
ATSAME54N20A	0x61840x02		
ATSAME53N20A	0x61830x02		
ATSAME53N19A	0x61830x03		
ATSAME53J18A	0x61830x06		
ATSAME53J19A	0x61830x05		
ATSAME53J20A	0x61830x04		
ATSAME51N19A	0x61810x01		
ATSAME51N20A	0x61810x00		
ATSAME51J18A	0x61810x03		
ATSAME51J19A	0x61810x02		
ATSAME51J20A	0x61810x04		
ATSAMD51P20A	0x60060x00		
ATSAMD51P19A	0x60060x01		
ATSAMD51N19A	0x60060x03		
ATSAMD51N20A	0x60060x02		
ATSAMD51J18A	0x60060x06		
ATSAMD51J19A	0x60060x05		
ATSAMD51J20A	0x60060x04		
ATSAMD51G18A	0x60060x08		
ATSAMD51G19A	0x60060x07		
ATSAME51G18A	0x61810306	N/A	0x3
ATSAME51G19A	0x61810305		

Data Sheet clarifications and corrections (if applicable) are located in the section Data Sheet Clarifications, following the discussion of silicon issues.

Note: Refer to the **"Device Service Unit"** chapter in the current preliminary device data sheet (DS60001507**F**) for a detailed information on Device Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Errata Summary

Table 1-1. Errata Summary

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A	D
Analog -to-Digital Converter(ADC)	ADC SYNCBUSY.SWTRIG	2.1.1	The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode.	X	X
Analog -to-Digital Converter(ADC)	ADC TUE/INL/DNL	2.1.2	The ADC TUE/INL/DNL performance is not guaranteed in the following scenarios: • Sampling frequency is above 500 ksps • ADC VREF is different from VDDANA	X	
Analog -to-Digital Converter(ADC)	Reference Buffer Offset Compensation	2.1.3	ADC converted data could be erroneous when using the Reference Buffer (REFCTRL.REFSEL =INTREF, INTVCC0, INTVCC1, VREFA or VREB) and when Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1).	X	X
Analog -to-Digital Converter(ADC)	DMA Sequencing	2.1.4	ADC DMA Sequencing with prescaler>8 (ADC->CTRLA.bit.PRESCALER>2), does not produce the expected channel sequence.	X	X
Analog -to-Digital Converter(ADC)	DMA Sequencing	2.1.5	ADC DMA Sequencing with averaging enabled (AVGCTRL.SAMPLENUM>1) without AVGCTRL bit set (DSEQCTRL.AVGCTRL=0) in the update sequence does not produce the expected channel sequence.	X	X
Analog Comparator (AC)	AC Hysteresis	2.2.1	Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which could result in unexpected behavior of the Analog Comparator.	X	X
Analog Comparator (AC)	Output	2.2.2	In continuous mode the Comparator output may toggle during startup time before the Ready Status bit is set (STATUSB.READY = 1).	X	X
Configurable Custom Logic (CCL)	Enable Protected Registers	2.3.1	The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they should be enable-protected by the LUTCTRLx.ENABLE bits.	X	X
Configurable Custom Logic (CCL)	Sequential Logic	2.3.2	LUT output is corrupted after enabling CCL when sequential logic is used.	X	X
Controller Area Network (CAN)	CAN Edge Filtering	2.4.1	When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does not correctly receive the first bit of the frame. In this case, the CRC will detect the first bit that was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send.	X	X
Controller Area Network (CAN)	Dominant Bit of Intermission	2.4.2	When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module.	X	X
Controller Area Network (CAN)	INTFLAG Status	2.4.3	Message transmitted with wrong arbitration and control fields.	X	X
Controller Area Network (CAN)	DAR Mode	2.4.4	Retransmission in DAR mode due to lost arbitration.	X	X
Controller Area Network (CAN)	High Priority Message (HPM) interrupt	2.4.5	Unexpected High Priority Message (HPM) interrupt	X	X
Controller Area Network (CAN)	TxFIFO	2.4.6	Tx FIFO message sequence inversion	X	X
Clock Failure Detector (CFD)	CFD with XOSC/XOSC32K Oscillator	2.5.1	When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail.	X	

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Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A	D
Device	Reverse Current in VDDIOB Domain	2.6.1	For the device with 100-pin, 120-pin, and 128-pin counts, when VDDIOB is supplied with the voltage less than VDDIO - 0.7V, reverse current in VDDIOB cluster is observed.	X	
Device	Internal Pull-up on the RESET Pin	2.6.2	The internal pull-up of the RESET pin is not functional.	X	
Device	Detection of a Debugger Probe	2.6.3	The detection of a debugger probe could fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled).	X	X
Device	VBAT Mode	2.6.4	VBAT mode is not functional.	X	
Device	Internal Reference	2.6.5	When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C.	X	
Device	Device Operation for Temperature < -20°C	2.6.6	If the operating temperature is less than -20°C, the device does not start.	X	X
Device Service Unit	CRC32	2.7.1	DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.	X	X
48 MHz Digital Frequency-Locked Loop (DFLL48M)	COARSE or FINE Calibration Values During the Locking Sequence	2.8.1	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X	X
48 MHz Digital Frequency-Locked Loop (DFLL48M)	STATUS.DFLLRDY Bit in Close Loop Mode	2.8.2	In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available.	X	X
48 MHz Digital Frequency-Locked Loop (DFLL48M)	DFLLVAL.FINE Value When DFLL48M Re-enabled	2.8.3	If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency.	X	
48 MHz Digital Frequency-Locked Loop (DFLL48M)	LLAW	2.8.4	When the Lose Lock After Wake (LLAW) is set, the DFLL may maintain lock (STATTUS.DFLLLOCK = 1) after the DFLL is disabled. If the DFLL lock (STATUS.DFLLLOCK = 1) is maintained when the DFLL is reconfigured and then enabled, some bits may not be properly set.	X	X
Digital-to-Analog Converter (DAC)	Differential Mode the Smoothing of the Output Signal	2.9.1	In Differential mode the smoothing of the output signal is not fully functional.	X	X
Digital-to-Analog Converter (DAC)	VDDANA as the DAC Reference	2.9.2	The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional.	X	
Digital-to-Analog Converter (DAC)	DAC on Negative Input AIN3	2.9.3	No analog compare will be done on Comparator 1 (AC1) when using the DAC on negative input AIN3.	X	
Digital-to-Analog Converter (DAC)	Interpolation Mode	2.9.4	If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, hence the DAC final output value does not correspond to the DAC input value.	X	X
Digital-to-Analog Converter (DAC)	Reference	2.9.5	The reference select of the DAC (CTRLB.REFSEL) will default to a '0' if the DAC Software Reset (CTRLA.SWRST) is used to reset the module.	X	X
Direct Memory Access Controller (DMAC)	Linked Descriptors	2.10.1	When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) could occur on enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled could be fetched by one of the already active channels using linked descriptors.	X	X
Direct Memory Access Controller (DMAC)	Channel Priority	2.10.2	When using channels with different priority levels, the highest priority channel could stall at the end of its current block.	X	
Direct Memory Access Controller (DMAC)	DMAC in Debug Mode	2.10.3	In debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN=0.	X	
Ethernet MAC (GMAC)	Ethernet Functionality in 64-pin Packages	2.11.1	Ethernet functionality in 64-pin packages is not available.	X	

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Module	Feature	Item Number	Issue Summary	Affected Revisions A	Affected Revisions D
External Interrupt Controller (EIC)	Edge Detection	2.12.1	When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).	X	X
External Interrupt Controller (EIC)	Asynchronous Edge Detection	2.12.2	When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.	X	X
Fractional Digital Phase-Locked Loop (FDPLL)	Low-Frequency Input Clock on FDPLLn	2.13.1	When using a low-frequency input clock (≤400kHz) on FDPLLn, several FDPLL unlocks could occur while the output frequency is stable.	X	X
Fractional Digital Phase-Locked Loop (FDPLL)	FDPLL Ratio in DPLLnRATIO	2.13.2	When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not beset when the ratio update will be completed.	X	X
Non-Volatile Memory Controller (NVMCTRL)	NVM Read Corruption	2.14.1	NVM reads could be corrupted when mixing NVM reads with Page Buffer writes.	X	X
Peripheral Access Controller (PAC)	PAC Protection Error in FREQM	2.15.1	FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.	X	X
Peripheral Access Controller (PAC)	PAC Protection Error in CCL	2.15.2	Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.	X	X
I/O Pin Controller (PORT)	PORT Read/Write Attempts on Non-Implemented Registers	2.16.1	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.	X	X
I/O Pin Controller (PORT)	PORT Pull-Up/Pull-Down Resistor	2.16.2	The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF.	X	
Real-Time Counter (RTC)	Write Corruption	2.17.1	A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers: • The COUNT register in COUNT32 mode • The COUNT register in COUNT16 mode • The CLOCK register in CLOCK mode	X	X
Real-Time Counter (RTC)	COUNTSYNC	2.17.2	When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and therefore it is a wrong value.	X	X
Real-Time Counter (RTC)	Tamper Input Filter	2.17.3	Majority debouncing, as part of RTC tamper detection, does not work, when enabled by setting Debouncer Majority Enable bit CTRLB.DEBMAJ.	X	X
Real-Time Counter (RTC)	Tamper Detection	2.17.4	Upon enabling the RTC, a false tamper detection could be reported by the RTC.	X	X
Real-Time Counter (RTC)	Tamper Detection Timestamp	2.17.5	If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.	X	X
Real-Time Counter (RTC)	PRESCALER	2.17.6	When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER=0).	X	X
Serial Communication Interface (SERCOM)	SERCOM-USART: USART Auto-Baud Mode	2.18.1	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X	X
Serial Communication Interface (SERCOM)	SERCOM-USART: Collision Detection	2.18.2	In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.	X	X
Serial Communication Interface (SERCOM)	SERCOM-USART: Debug Mode	2.18.3	In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.	X	X

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Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A	D
Serial Communication Interface (SERCOM)	SERCOM-USART: 32-bit Extension Mode	2.18.4	When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes (which means the length counter must be enabled), additional bytes will be sent over the line.	X	X
Serial Communication Interface (SERCOM)	SERCOM-UART: TXINV and RXINV Bits	2.18.5	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	X	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: SDAHOLD Timing	2.18.6	SDAHOLD timing of the SERCOM-I^2C does not match the value shown in the current device data sheet.	X	X
Serial Communication Interface (SERCOM)	Repeated Start in High-Speed Master Write Operation	2.18.7	For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.	X	X
Serial Communication Interface (SERCOM)	Repeated Start in High-Speed Master Read Operation	2.18.8	For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.	X	X
Serial Communication Interface (SERCOM)	STATUS.CLKHOLD Bit in Master and Slave Modes	2.18.9	The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.	X	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: I^2C in Slave Mode	2.18.10	In I^2C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.	X	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: Slave Mode with DMA	2.18.11	In I^2C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register.	X	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: I^2C Slave in DATA32B Mode	2.18.12	When SERCOM is configured as an I^2C slave in 32-bit Data Mode (DATA32B=1) and the I^2C master reads from the I^2C slave (slave transmitter) and outputs its NACK (indicating no more data is needed), the I^2C slave still receives a DRDY interrupt.	X	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: 10-bit Addressing Mode	2.18.13	10-bit addressing in I^2C Slave mode is not functional.	X	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: Repeated Start	2.18.14	When the Quick command is enabled (CTRLB.QCEN=1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields.	X	X
Serial Communication Interface (SERCOM)	SERCOM-SPI: Data Preload	2.18.15	In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.	X	X
Serial Communication Interface (SERCOM)	Repeated Start	2.18.16	For Master Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue correctly a Repeated Start command.	X	X
Serial Communication Interface (SERCOM)	Wakeup	2.18.17	The USART does not wake-up the device on Error (INTFLAG.ERROR=1) interrupt.	X	X
Serial Communication Interface (SERCOM)	LENGTH	2.18.18	When the USART is used in 32-bit mode with hardware handshaking (CTS/RTS) the TXC interrupt flag (INTFLAG.TXC) may be set before transmission has completed. The TXC interrupt flag may incorrectly be set regardless of Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.	X	X
Serial Communication Interface (SERCOM)	USART	2.18.19	Unexpected over-consumption in standby mode	X	X
Supply Controller (SUPC)	Buck Converter Mode	2.19.1	Digital Phase-Locked Loop (FDPLL200Mx2) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode.	X	X
Supply Controller (SUPC)	BOD33 Hysteresis	2.19.2	The hysteresis feature of the 3.3V BOD is not functional while the device is in STANDBY sleep mode.	X	X

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Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A	D
Timer/Counter (TC)	PERBUF/CCBUFx Register	2.20.1	When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.	X	X
Timer/Counter for Control Applications (TCC)	TCC with EVSYS in SYNC/ RESYNC Mode	2.21.1	TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.	X	X
Timer/Counter for Control Applications (TCC)	Dithering Mode with External Retrigger Events	2.21.2	Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right aligned pulses, or shrink of left-aligned pulses.	X	X
Timer/Counter for Control Applications (TCC)	ALOCK Feature	2.21.3	ALOCK feature is not functional.	X	X
Timer/Counter for Control Applications (TCC)	LUPD feature in Down-Counting mode	2.21.4	In down-counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.	X	X
Reserved	-	2.22.1	-		
Voltage Reference System	Temperature sensor	2.23.1	Temperature sensors are not supported.	X	X

Note:
- Cells with ‘X’ indicates the issue is present in this revision of the silicon.
- Cells with ‘-’ indicates this silicon revision does not exist for this issue.
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon.

2. Silicon Errata Issues

The following errata issues apply to the SAM D5x/E5x family of devices.

Note:
Cells with an ‘X’ indicates the issue is present in this revision of the silicon.

Cells with a dash (‘-’) indicate this silicon revision does not exist for this issue.

Blank cells indicate the issue has been corrected or does not exist in this revision of the silicon.

2.1 Analog-to-Digital Converter (ADC)

2.1.1 ADC SYNCBUSY.SWTRIG

The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode.

Workaround
Ignore the ADC SYNCBUSY.SWTRIG status when waking up from Sleep mode.

Affected Silicon Revisions

A	D						
X	X						

2.1.2 ADC TUE/INL/DNL Performance

The ADC TUE/INL/DNL performance is not guaranteed in the following scenarios:

- Sampling frequency is above 500 ksps AND
- ADC V_{REF} is different from VDDANA

Workaround
None.

Affected Silicon Revisions

A	D						
X							

2.1.3 Reference Buffer Offset Compensation

ADC converted data could be erroneous when using the Reference Buffer (REFCTRL.REFSEL = INTREF, INTVCC0, INTVCC1, VREFA or VREB) and when Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1).

Workaround
The first five conversions must be ignored. All further ADC module conversions are accurate.

Affected Silicon Revisions

A	D						
X	X						

2.1.4 DMA Sequencing

ADC DMA Sequencing with prescaler > 8 (ADC->CTRLA.bit.PRESCALER>2) does not produce the expected channel sequence.

Workaround
Keep the prescaler setting to a maximum of 8, and use the GCLK Generator divider if more prescaling is needed.

Affected Silicon Revisions

A	D						
X	X						

2.1.5 DMA Sequencing

ADC DMA sequencing with averaging enabled (AVGCTRL.SAMPLENUM>1) without the AVGCTRL bit set (DSEQCTRL.AVGCTRL= 0) in the update sequence does not produce the expected channel sequence.

Workaround
Add the AVGCTRL register in the register update list (DSEQCTRL.AVGCTRL= 1) and set the desired value in this list.

Affected Silicon Revisions

A	D						
X	X						

2.2 Analog Comparator (AC)

2.2.1 AC Hysteresis

Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which could result in unexpected behavior of the Analog Comparator.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.2.2 Output

In Continuous mode the comparator output may toggle during startup time before the Ready Status bit is set (STATUSB.READY = 1).

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.3 Configurable Custom Logic (CCL)

2.3.1 Enable Protected Registers

The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they must be enable-protected by the LUTCTRLx.ENABLE bits.

Workaround

None.

Affected Silicon Revisions

A	D						
X	X						

2.3.2 Sequential Logic Reference

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround

Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

A	D						
X	X						

2.4 Controller Area Network (CAN)

2.4.1 CAN Edge Filtering

When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does not correctly receive the first bit of the frame. In this case, the CRC will detect the first bit that was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send.

The issue only occurs when there is a falling edge at the Rx input pin (CAN_RX) within the last time quantum (tq) before the end of the integration phase. The last time quantum of the integration phase is at the sample point of the 11th recessive bit of the integration phase. When edge filtering is enabled, the bit timing logic of the CAN sees the Rx input signal delayed by the edge filtering. When the integration phase ends, edge filtering is automatically disabled. This affects the reset of the FD CRC registers at the beginning of the frame. The Classical CRC register is not affected, hence this issue does not affect the reception of Classical frames.

In CAN communication, the CAN module may enter an integrating state (either by resetting the CCCR.INIT or by protocol exception event) while a frame is active on the bus. In this case, the 11 recessive bits are counted between the acknowledge bit and the following start of frame. All nodes have synchronized at the beginning of the dominant acknowledge bit. This means that the edge of the following start of frame bit cannot fall on the sample point, hence the issue does not occur. The issue occurs only when the CAN is by local errors, mis-synchronized with regard to the other nodes.

Glitch filtering as specified in ISO 11898-1:2015 is fully functional.

Edge filtering was introduced for applications where the data bit time is at least 2-tq (of nominal bit time) long. In that case, edge filtering requires at least two consecutive dominant time quanta before the counter counting the 11 recessive bits for idle detection is restarted. This means edge filtering covers the theoretical case of occasional 1-tq long dominant spikes on the CAN bus that would delay idle detection. Repeated dominant spikes on the CAN bus would disturb all CAN communication, so the filtering to speed up idle detection would not help network performance.

When this rare event occurs, the CAN sends an error frame and the sender of the affected frame retransmits the frame. When the retransmitted frame is received, the CAN has left the integration phase and the frame will be received correctly. Edge filtering is only applied during the integration phase and it is never used during normal operation. Because the integration phase is very short with respect to "active communication time", the impact on total error frame rate is negligible. The issue has no impact on data integrity.

The CAN enters the integration phase under the following conditions:

- When CCCR.INIT is set to '0' after start-up
- After a protocol exception event (only when CCCR.PXHD = 0)

Scope:

The erratum is limited to FD frame reception when edge filtering is active (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin.

Effects:

The calculated CRC value does not match the CRC value of the received FD frame and the CAN module sends an error frame. After retransmission the frame is received correctly.

Workaround:

Disable edge filtering or wait on retransmission in the event that this rare event occurs.

Affected Silicon Revisions

A	D						
X	X						

2.4.2 Dominant Bit of Intermission

When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module.

Workaround

A phase buffer segment 2 of length '1' (Phase_Seg2(N) = 1) is not sufficient to switch to the first identifier bit after the sample point in intermission where the dominant bit was detected.

The CAN protocol according to ISO 11898-1 defines that a dominant third bit of intermission causes a pending transmission to be started immediately. The received dominant bit is handled as if the CAN has transmitted a Start-of-Frame (SoF) bit.

The ISO 11898-1 specifies the minimum configuration range for Phase_Seg2(N) to be 2..8 tq. Therefore, excluding a Phase_Seg2(N) of '1' will not affect CAN conformance.

Effects:

If NBTP.NTSEG2 = 0, it may occur that the CAN transmits the first identifier bit dominant instead of recessive.

Update configuration range of NBTP.NTSEG2 from 0..127 tq to 1..127 tq in the CAN documentation.

Affected Silicon Revisions

A	D						
X	X						

2.4.3 Message Transmitted with Wrong Arbitration and Control Fields

Description:

Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- The CAN is in the "Receiver" (PSR.ACT ≠0b10) state, hence no pending transmission

- A new transmission is requested before the third bit of intermission is reached
- The CAN bus is sampled dominant at the third bit of intermission which is treated as SoF (See ISO11898-1:2015, “Section 10.4.2.2”)

Under the conditions above, the following might happen:

- The shift register is not loaded with ID, format, and DLC of the requested message
- The CAN will start arbitration with wrong ID, format, and DLC on the next bit
- If the ID wins arbitration, a CAN message with a valid CRC is transmitted
- If this message is acknowledged, the ID stored in the Tx event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, hence no error is detected by the transmitting CAN

Scope:

The erratum is limited when CAN is in the "Receiver" (PSR.ACT = 0b10) state with no pending transmission (register TXBRP == 0) and a new transmission is requested before the third bit of intermission is reached and this third bit of intermission is seen dominant.

When a transmission is requested by the CPU by writing to TXBAR, the Tx message handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated in the critical time window between the sample points of the second and third bit of intermission and if that third bit of intermission is seen dominant.

This dominant level at the third bit of intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

Effects:

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

Workarounds

- **Workaround 1:** Request a new transmission only if another transmission is already pending (that is, register TXBRP ≠ 0) or when the CAN is not in the "Receiver" (when PSR.ACT ≠ 0b10) state. To avoid activating the transmission request in the critical time window between the sample points of the second and third bit of intermission, the application software can evaluate the Rx interrupt flags, such as IR.DRX, IR.RF0N, and IR.RF1N, which are set at the last bit of EoF when a received and accepted message becomes valid. The last bit of EoF is followed by third bits of intermission. Therefore the critical time window has safely terminated three bit times after the Rx interrupt. Now a transmission may be requested by writing to TXBAR. After the interrupt, the application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.
- **Workaround 2:** If a transmission is to be requested while no other transmission request is already pending and the CAN bus is not idle, set the CCCR.INIT bit (which stops the CAN protocol controller), set the transmission request and clear the CCCR.INIT bit. The message currently being received when the CCCR.INIT bit is set will be lost, but no errors (or error frames) will be generated and the CAN protocol controller will re-integrate into the CAN communication immediately at the 11 recessive bits of the next End-of-Frame including intermission.
- **Workaround 3:**It is also possible to keep the number of pending transmissions always at > 0 by frequently requesting a message, then the condition "no pending transmission" is never met. The frequently requested message may be given a low priority, losing arbitration to all other messages.

Affected Silicon Revisions

A	D						
X	X						

2.4.4 DAR Mode

When the CAN is configured in DAR mode (CCCR.DAR = 1) the automatic retransmission for transmitted messages that have been disturbed by an error or have lost arbitration is disabled. When the transmission attempt is not successful, the Tx Buffer's Transmission Request bit (TXBRP.TRPn) will be cleared and the Tx Buffer's Cancellation Finished bit (TXBCF.CFn) will be set.

When the transmitted message loses arbitration at one of the first two identifier bits, chances are that instead of the bits of the actually transmitted Tx Buffer, the TXBRP.TRPn and TXBCF.CFn bits of the previously started Tx Buffer (or Tx Buffer 0 if there is no previous transmission attempt) are written (TXBRP.TRPn = 0, TXBCF.CFn = 1).

If in this case the TXBRP.TRPn bit of the Tx Buffer that lost arbitration at the first two identifier bits are not cleared, retransmission is attempted. When the CAN loses arbitration again at the immediately following retransmission, then actually and previously transmitted Tx Buffer are the same and this Tx Buffer's TXBRP.TRPn bit is cleared and its TXBCF.CFn bit is set.

Scope:

The erratum is limited to the case when the CAN loses arbitration at one of the first two transmitted identifier bits while in DAR mode. The problem does not occur when the transmitted message is disturbed by an error.

Effects:

In this case, it might happen that the TXBRP.TRPn bit is cleared after the second transmission attempt instead of the first. Additionally it may happen that the TXBRP.TRPn bit of the previously started Tx Buffer is cleared, if it has been set again. As in this case the previously started Tx Buffer has lost CAN internal arbitration against the active Tx Buffer, its message has a lower identifier priority. It would also have lost arbitration on the CAN bus at the same position.

Workaround

None.

Affected Silicon Revisions

A	D						
X	X						

2.4.5 High-Priority Message (HPM) interrupt

There are two configurations where the issue occurs:

Configuration A:

- At least one Standard Message ID Filter Element is configured with priority flag set (S0.SFEC = 0b100/0b101/0b110)
- No Extended Message ID Filter Element configured
- Non-matching extended frames are accepted (GFC.ANFE = 0b00/0b01)

The HPM interrupt flag IR.HPM is set erroneously on reception of a non-high-priority extended message under the following conditions:

1. A standard HPM frame is received and accepted by a filter with priority flag set (that is, Interrupt flag IR.HPM is set as expected).
2. An extended frame is received and accepted because of the GFC.ANFE configuration (that is, Interrupt flag IR.HPM is set erroneously).

Configuration B:

- At least one Extended Message ID filter element is configured with priority flag set (F0.EFEC = 0b100/0b101/0b110)
- No Standard Message ID filter element is configured
- Non matching standard frames are accepted (GFC.ANFS = 0b00/0b01)

The HPM interrupt flag IR.HPM is set erroneously on reception of a non high-priority standard message under the following conditions:

1. An extended HPM frame is received and accepted by a filter with priority flag set (that is, Interrupt flag IR.HPM is set as expected).
2. A standard frame is received and accepted because of the GFC.ANFS configuration (that is, Interrupt flag IR.HPM is set erroneously).

Scope:

The erratum is limited to the following configurations:

Configuration A:

No Extended Message ID filter element is configured and non matching extended frames are accepted due to Global Filter Configuration (GFC.ANFE = 0b00/0b01).

Configuration B:

No Standard Message ID Filter Element configured and non-matching standard frames are accepted due to Global Filter Configuration (GFC.ANFS = 0b00/0b01).

Effects:

Interrupt flag IR.HPM is set erroneously at the reception of a frame with:

- Configuration A: Extended Message ID
- Configuration B: Standard Message ID

Workaround
Configuration A:

Setup an Extended Message ID filter element with the following configuration:

- F0.EFEC = 001/010: Select Rx FIFO for storage of extended frames
- F0.EFID1 = any value: The value is not relevant as all ID bits are masked out by F1.EFID2
- F1.EFT = 10: Classic filter, F0.EFID1 = filter, F1.EFID2 = mask
- F1.EFID2 = 0: All bits of the received extended ID are masked out

Now all extended frames are stored in Rx FIFO ‘0’ or Rx FIFO ‘1’ depending on the configuration of F0.EFEC.

Configuration B:

Setup an Standard Message ID filter element with the following configuration:

- S0.SFEC = 001/010: Select Rx FIFO for storage of standard frames
- S0.SFID1 = any value: The value is not relevant as all ID bits are masked out by S0.SFID2
- S0.SFT = 10: Classic filter, S0.SFID1 = filter, S0.SFID2 = mask
- S0.SFID2 = 0: All bits of the received standard ID are masked out

Now all standard frames are stored in Rx FIFO ‘0’ or Rx FIFO ‘1’ depending on the configuration of S0.SFEC.

Affected Silicon Revisions

A	D						
X	X						

2.4.6 Tx FIFO message sequence inversion

Assuming that there are two Tx FIFO messages in the output pipeline of the Tx Message Handler. Transmission of Tx FIFO message 1 is started:

Position 1: Tx FIFO message 1 (transmission ongoing)

Position 2: Tx FIFO message 2

Position 3: Free FIFO bugger

During the transmission of Tx FIFO message 1, a non Tx FIFO message with a higher CAN priority is requested. Due to its priority it will be inserted into the output pipeline. The TxMH performs "message scans" to keep the output pipeline up to date with the highest priority messages from the message RAM.

After the following two message scans, the output pipeline has the following content:

Position 1: Tx FIFO message 1 (transmission ongoing)

Position 2: non Tx FIFO message with higher CAN priority

Position 3: Tx FIFO message 2

If the transmission of Tx FIFO message 1 is not successful (lost arbitration or CAN bus error) it is pushed from the output pipeline by the non Tx FIFO message with higher CAN priority. The following scan again inserts Tx FIFO message 1 into the output pipeline at position 3:

Position 1: non Tx FIFO message with higher CAN priority (transmission ongoing)

Position 2: Tx FIFO message 2

Position 3: Tx FIFO message 1

This results in Tx FIFO message 2 being in the output pipeline in front of Tx FIFO message 1 and they are transmitted in that order, resulting in a message sequence inversion.

Scope:

The erratum describes the case when the CAN uses both, dedicated Tx Buffers and a Tx FIFO (TXBC.TFQM = 0) and the messages in the Tx FIFO do not have the highest internal CAN priority. The described sequence inversion may also happen between two non Tx FIFO messages (Tx Queue or dedicated Tx Buffers) that have the same CAN identifier and that should be transmitted in the order of their buffer numbers (not the intended use).

Effects:

In the described case it may happen that two consecutive messages from the Tx FIFO exchange their positions in the transmit sequence.

Workarounds

When transmitting messages from a dedicated Tx Buffer with higher priority than the messages in the Tx FIFO, choose one of the following workarounds:

Workaround 1

Use two dedicated Tx Buffers, for example, use Tx Buffers 4 and 5 instead of the Tx FIFO.

The Transmit Loop below replaces the function that fills the Tx FIFO.

Write the message to Tx Buffer 4

Transmit Loop:

- Request Tx Buffer 4 - write TXBAR.A4
- Write message to Tx Buffer 5
- Wait until transmission of Tx Buffer 4 completed - IR.TC, read TXBTO.TO4
- Request Tx Buffer 5 - write TXBAR.A5
- Write message to Tx Buffer 4
- Wait until transmission of Tx Buffer 5 completed - IR.TC, read TXBTO.TO5

Workaround 2

Ensure that only one Tx FIFO element is pending for transmission at any time.

The Tx FIFO elements may be filled at any time with messages to be transmitted, but their transmission requests are handled separately. Each time a Tx FIFO transmission has completed and the Tx FIFO becomes empty (IR.TFE = 1), the next Tx FIFO element is requested.

Workaround 3

Use only a Tx FIFO. Send the message with the higher priority also from Tx FIFO.

Drawback: The higher priority message has to wait until the preceding messages in the Tx FIFO are sent.

Affected Silicon Revisions

A	D						
X	X						

2.5 Clock Failure Detector (CFD)

2.5.1 CFD with XOSC/XOSC32K Oscillator

When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail.

Workaround

Two possible workarounds are as follows:

1. If the main clock source comes from the XOSC/XOSC32K oscillator, the only workaround is indirect (i.e., using the WDT in firmware and switch to safe clock source in firmware at WDT reset).
2. Because the clock failure detection is functional, once the STATUS.CLKFAIL is set, and if the STATUS.CLKSW is not set, manually switch to safe clock from firmware by changing the configurations of the Generic Clock Generators that use the XOSC/XOSC32K oscillator as a clock source to use another source clock instead.

Affected Silicon Revisions

A	D						
X							

2.6 Device

2.6.1 Reverse Current in VDDIOB Domain

For the device with 100-pin, 120-pin, and 128-pin counts, when VDDIOB is supplied with the voltage less than VDDIO - 0.7V, reverse current in VDDIOB cluster is observed.

Workaround

None. Pin PB13 must be tied to ground.

Affected Silicon Revisions

A	D						
X							

2.6.2 Internal Pull-up on the RESET Pin

The internal pull-up of the RESET pin is not functional.

Workaround

An external 100K pull-up must be added on the RESET pin.

Affected Silicon Revisions

A	D						
X							

2.6.3 Detection of a Debugger Probe

The detection of a debugger probe could fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled).

Workaround
To secure the detection of debugger probes, enable BOD33 using the SUPC.BOD33 register instead of the "BOD33 Disable" fuse. The "BOD33 Disable" fuse must be kept set.

Affected Silicon Revisions

A	D						
X	X						

2.6.4 VBAT Mode

V_{BAT} mode is not functional.

Workaround
None.

Affected Silicon Revisions

A	D						
X							

2.6.5 Internal Reference

When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C.

Workaround
The internal reference must be used only for positive temperatures (i.e., above 0°C).

Affected Silicon Revisions

A	D						
X							

2.6.6 Device Operation for Temperature < -20°C

If the operating temperature is less than -20°C, the device does not start.

Workaround
Apply an external reset pulse at power-up when V_{DD} is higher than 2V, or keep reset line low until V_{DD} is lower than 2V.

Affected Silicon Revisions

Device	A	D					
Package Grade U with EFP	-						

...........continued

Device	A	D					
Package Grade U without EFP	X	X					
Other Package Grades	X						

Note: EFP refers to Extended Flash Performance and is only available for package grade U = -40°C to +85°C Matte Sn Plating (Industrial). For additional information, refer to the device data sheet.

2.7 Device Service Unit (DSU)

2.7.1 CRC32

The DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.

Workaround
Be sure to always enable the NVM cache when performing a DSU CRC32 request targeting the NVM memory space.

Affected Silicon Revisions

A	D						
X	X						

2.8 48 MHz Digital Frequency-Locked Loop (DFLL48M)

2.8.1 COARSE or FINE Calibration Values During the Locking Sequence

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround
Check that lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

A	D						
X	X						

2.8.2 STATUS.DFLLRDY Bit in Close Loop Mode

In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.8.3 DFLLVAL.FINE Value When DFLL48M Re-enabled

If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency.

Workaround
Before writing the final configuration in the DFLLCTRLB register, the DFLL module must be re-enabled in Open Loop mode to read and rewrite the DFLLVAL register.

1. `OSCCTRL->DFLLMUL.reg = X; // Write new DFLLMULL configuration`
2. `OSCCTRL.DFLLCTRLB.reg = 0; // Select Open loop configuration`
3. `OSCCTRL.DFLLCTRLA.bit.ENABLE = 1; // Enable DFLL`
4. `OSCCTRL.DFLLVAL.reg = OSCCTRL->DFLLVAL.reg; // Reload DFLLVAL register`
5. `OSCCTRL.DFLLCTRLB.reg = X; // Write final DFLL configuration`

Affected Silicon Revisions

A	D						
X							

2.8.4 LLAW

When the Lose Lock After Wake (LLAW) is set, the DFLL may maintain lock (STATTUS.DFLLLOCK = 1) after the DFLL is disabled. If the DFLL lock (STATUS.DFLLLOCK = 1) is maintained when the DFLL is reconfigured and then enabled, some bits may not be properly set.

Workaround
When reconfiguring the DFLL wait for the lock status to set to ‘0’ (STATUS.DFLLLOCK = 0) after disabling the DFLL (DFLLCTRLA.ENABLE = 0).

Affected Silicon Revisions

A	D						
X	X						

2.9 Digital-to-Analog Converter (DAC)

2.9.1 Smoothing of the Output Signal in differential Mode

In Differential mode the smoothing of the output signal is not fully functional. Smoothing works normally in Differential mode as long as the value of two consecutive data are both positive or negative. The behavior is incorrect when the data changes from positive to negative or vice versa.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.9.2 VDDANA as the DAC Reference

The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional.

Workaround
The VDDANA must be connected externally to a V_{REF} pin and DAC.CTRLB.VREFAU must be selected.

Affected Silicon Revisions

A	D						
X							

2.9.3 DAC on Negative Input AIN3

No analog compare will be done on Comparator 1 (AC1) when using the DAC on negative input AIN3.

Workaround
Use the internal VDD scaler.

Affected Silicon Revisions

A	D						
X							

2.9.4 Interpolation Mode

If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, and therefore, the DAC final output value does not correspond to the DAC input value.

Although interrupt events are generated at the end of conversion (EOC), the EOC occurs before the final value from the filter and is of no use in the application.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.9.5 Reference

The reference select of the DAC (CTRLB.REFSEL) will default to a ‘0’ if the DAC Software Reset (CTRLA.SWRST) is used to reset the module.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.10 Direct Memory Access Controller (DMAC)

2.10.1 Linked Descriptors

When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) could occur on enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled could be fetched by one of the already active channels using linked descriptors. These errors can occur when a channel is being enabled during the link request of another channel and if the channel number of the channel being enabled is lower than the channel already active.

Workaround
When enabling a channel while other channels using linked descriptors are already active, the channel number of the new channel to enable must be greater than the other channel numbers.

Affected Silicon Revisions

A	D						
X	X						

2.10.2 Channel Priority

When using channels with different priority levels, the highest priority channel could stall at the end of its current block.

When this occurs, the channel is seen as active with BTCNT = 0 in the ACTIVE register with Busy and Pending flag set in the CHSTATUSn register. This condition also prevents the other channels from executing.

Workaround
None.

Affected Silicon Revisions

A	D						
X							

2.10.3 DMAC in Debug Mode

In Debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN = 0.

Workaround
Set DBGCTRL.DBGRUN to 1 so that the DMAC continues normal operation when the CPU is halted by an external debugger.

Affected Silicon Revisions

A	D						
X							

2.11 Ethernet MAC (GMAC)

2.11.1 Ethernet Functionality in 64-pin Packages

Ethernet functionality in 64-pin packages is not available.

Workaround
None.

Affected Silicon Revisions

A	D						
X							

2.12 External Interrupt Controller (EIC)

2.12.1 Edge Detection

When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.12.2 Asynchronous Edge Detection

When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

Workaround
Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

Affected Silicon Revisions

A	D						
X	X						

2.13 Fractional Digital Phase-Locked Loop (FDPLL)

2.13.1 Low-Frequency Input Clock on FDPLLn

When using a low-frequency input clock (≤ 400 kHz) for input to FDPLLn, several FDPLL false unlock status indications may occur while the FDPLL output frequency is actually stable.

Workaround
When using a low-frequency input clock (≤ 400 kHz) on FDPLLn, enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) and wake up fast (OSCCTRL.DPLLCTRLB.WUF = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications but it disables the gating of the FDPLL clock output by the lock status; therefore, the clock is issued even if the FDPLL status shows unlocked. The Clock Ready bit (OSCCTRL.DPLLSTATUS.CLKRDY) can be monitored by the application to ensure activity is present on the FDPLLn output, but clock ready does not provide any indication of FDPLLn Lock or frequency. A 10 ms delay is also suggested after the clock ready bit is set to allow the DPLL to achieve the target frequency.

Pseudo Code

Set OSCCTRL.DPLLCTRLB.WUF = 1 and OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY == 1)

Delay (10ms)

Set Source for GCLK with DPLL

Affected Silicon Revisions

A	D						
X	X						

2.13.2 FDPLL Ratio in DPLLnRATIO

When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.

Workaround
Wait for the interruption flag INTFLAG.DPLLnLDRTO instead.

Affected Silicon Revisions

A	D						
X	X						

2.14 Non-Volatile Memory Controller (NVMCTRL)

2.14.1 NVM Read Corruption

NVM reads could be corrupted when mixing NVM reads with Page Buffer writes.

Workaround
Disable cache lines before writing to the Page Buffer when executing from NVM or reading data from NVM while writing to the Page Buffer. Cache lines are disabled by writing a one to CTRLA.CACHEDIS0 and CTRLA.CACHEDIS1.

Affected Silicon Revisions

A	D						
X	X						

2.15 Peripheral Access Controller (PAC)

2.15.1 PAC Protection Error in FREQM

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.15.2 PAC Protection Error in CCL

Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.

Workaround
Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

A	D						
X	X						

2.16 I/O Pin Controller (PORT)

2.16.1 PORT Read/Write Attempts on Non-Implemented Registers

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.16.2 PORT Pull-Up/Pull-Down Resistor

The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF.

Workaround
None.

Affected Silicon Revisions

A	D						
X							

2.17 Real-Time Counter (RTC)

2.17.1 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode

- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround
Write the registers with:

- A 32-bit write access for COUNT register in COUNT32 mode, CLOCK register in CLOCK mode
- A 16-bit write access for the COUNT register in COUNT16 mode

Affected Silicon Revisions

A	D						
X	X						

2.17.2 COUNTSYNC

When COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and thus it is a wrong value.

Workaround
After enabling COUNTSYNC, read the COUNT register until its value is changed when compared to its first value read. After this, all consequent value read from the COUNT register is valid.

Affected Silicon Revisions

A	D						
X	X						

2.17.3 Tamper Input Filter

Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit, CTRLB.DEBMAJ.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.17.4 Tamper Detection

Upon enabling the RTC tamper detection feature, a false tamper detection can be reported by the RTC.

Workarounds
Use any one of the following workarounds:

- **Workaround 1**: Configure TAMPER detection as ONLY falling edge.
- **Workaround 2**: If the user software has to use TAMPER detection as rising edge, it must ignore the first tamper interrupt generated immediately after enabling the RTC tamper detection.

Affected Silicon Revisions

A	D						
X	X						

2.17.5 Tamper Detection Timestamp

If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.

Workarounds

Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK register to one of the following destinations::

- SRAM
- GPx register in RTC
- BKUPx register in RTC

Affected Silicon Revisions

A	D						
X	X						

2.17.6 Prescaler

When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER = 0).

Workarounds

When the prescaler is OFF (CTRLA.PRESCALER = 0), clear the Periodic Interval n Event Output Enable bits (EVCTRL.PEREOn = 0 [n = 7...0]) and respective Periodic Interval n Interrupt Enable (INTENCLR.PERn = 1 [n = 7...0]) bits.

Affected Silicon Revisions

A	D						
X	X						

2.18 Serial Communication Interface (SERCOM)

2.18.1 SERCOM-USART: Auto-Baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround

None.

Affected Silicon Revisions

A	D						
X	X						

2.18.2 SERCOM-USART: Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Workaround

The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection. .

Affected Silicon Revisions

A	D						
X	X						

2.18.3 SERCOM-USART: Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted after entering Debug mode.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.18.4 SERCOM-USART: 32-bit Extension Mode

When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes, which means the length counter must be enabled, and additional bytes will be sent over the line.

Workarounds
Use any one of the following workarounds:
1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use length counter in firmware by keeping the data to be sent is in multiples of 4 bytes.

Affected Silicon Revisions

A	D						
X	X						

2.18.5 SERCOM-UART: TXINV and RXINV Bits

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

Workaround
In software interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

A	D						
X	X						

2.18.6 SERCOM-I²C: SDAHOLD Timing

SDAHOLD timing of the SERCOM-I²C does not match the value shown in the current device data sheet. The following table shows the specified and real values of SDA Hold timing.

Table 2-1. SDA Hold Timing

SDA Hold Time Value	Specified SDA Hold Time	Real SDA Hold Time
0x0	Disabled	Disabled
0x1	50 ns to 100 ns	20 ns to 40 ns

...........continued		
SDA Hold Time Value	**Specified SDA Hold Time**	**Real SDA Hold Time**
0x2	300 ns to 600 ns	100 ns to 250 ns
0x3	400 ns to 800 ns	150 ns to 350 ns

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.18.7 Repeated Start in High-Speed Master Write Operation

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.18.8 Repeated Start in High-Speed Master Read Operation

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.18.9 STATUS.CLKHOLD Bit in Master and Slave Modes

The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.

Workaround
Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A	D						
X	X						

2.18.10 SERCOM-I^{2}C: I^{2}C in Slave Mode

In I^{2}C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

Workaround
Manually clear status bits LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to 1 when set.

Affected Silicon Revisions

A	D						
X	X						

2.18.11 SERCOM-I^{2}C: Slave Mode with DMA

In I^{2}C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I ^{2}C bus will not occur causing the loss of this data.

Workaround
Configure the DMA transfer size to the number of data to be received by the I^{2}C master. DMA cannot be used if the number of data to be received by the master is not known..

Affected Silicon Revisions

A	D						
X	X						

2.18.12 SERCOM-I^{2}C: I^{2}C Slave in DATA32B Mode

When SERCOM is configured as an I^{2}C slave in 32-bit Data Mode (DATA32B = 1) and the I^{2}C master reads from the I^{2}C slave (slave transmitter) and outputs its NACK (indicating no more data is needed), the I^{2}C slave still receives a DRDY interrupt.

If the CPU does not write a new data to the I^{2}C slave DATA register, I^{2}C slave will pull SDA line, which will result in stalling the bus permanently.

Workarounds
1. Write a dummy data to data register when a NACK is received from the master.
2. Use command #2 (SERCOMx->I2CS.CTRLB.bit.CMD = 2) when a NACK is received from the master.

Important: Because STATUS.RXNACK always indicates the last received ACK, to determine when a NACK is received from the I^{2}C master, the I^{2}C slave software needs to consider I2CS.STATUS.RXNACK only on the second DRDY interrupt after receiving the AMATCH interrupt.

Affected Silicon Revisions

A	D						
X	X						

2.18.13 SERCOM-I^{2}C: 10-bit Addressing Mode

10-bit addressing in I^{2}C Slave mode is not functional.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.18.14 SERCOM-I^{2}C: Repeated Start

When the Quick command is enabled (CTRLB.QCEN = 1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround

Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch Mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

A	D						
X	X						

2.18.15 SERCOM-SPI: Data Preload

In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.

Workarounds

In SPI Slave mode, the Slave Select pin (SS) must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

A	D						
X	X						

2.18.16 SERCOM I^{2}C: Repeated Start

For Master Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue a Repeated Start command correctly.

Workarounds

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate properly a Repeated Start.

Affected Silicon Revisions

A	D						
X	X						

2.18.17 Wakeup

The USART does not wake-up the device on Error Interrupt (INTFLAG.ERROR = 1).

Workarounds

Configure the USART to wake-up the device on the RX Complete Interrupt (INTENSET.RXC = 1) in order to check the PERR/FERR status (STATUS.PERR = 1 or STATUS.FERR = 1).

Affected Silicon Revisions

A	D						
X	X						

2.18.18 LENGTH

When the USART is used in 32-bit mode with hardware handshaking (CTS/RTS), the TXC interrupt flag (INTFLAG.TXC) may be set before transmission has completed. The TXC interrupt flag may incorrectly be set regardless of Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.

Workarounds
None.

Affected Silicon Revisions

A	D						
X	X						

2.18.19 USART

When SERCOM USART CTRLA.RUNSTDBY= 0 and the Receiver is disabled (CTRLB.RXEN= 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected over-consumption.

Workarounds
Configure CTRLA.RXPO and CTRLA.TXPO in order to use the same SERCOM PAD for RX and TX or add an external pull-up on the RX pin.

Affected Silicon Revisions

A	D						
X	X						

2.19 Supply Controller (SUPC)

2.19.1 Buck Converter Mode

Buck Converter mode is not supported when using PLLs. As a result, the information given in Table 54-9 “Active Current Consumption - Active Mode” data for Buck converter mode with FDPLL and DFLL configurations is not valid and must be disregarded.

Workaround
Use the LDO Regulator mode when using FDPLL and DFLL configurations.

Affected Silicon Revisions

A	D						
X	X						

2.19.2 BOD33 Hysteresis

The hysteresis feature of the 3.3V BOD is not functional while the device is in STANDBY sleep mode.

Workaround
None.

Affected Silicon Revisions

A	D						
X	X						

2.20 Timer/Counter (TC)

2.20.1 PERBUF/CCBUFx Register

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

Workaround
Clear successively twice the STATUS.PERBUFV/STATUS.CCBUFx flag to ensure that the PERBUF/CCBUFx register value is restored before updating it.

Affected Silicon Revisions

A	D						
X	X						

2.21 Timer/Counter for Control Applications (TCC)

2.21.1 TCC with EVSYS in SYNC/RESYNC Mode

TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Workaround
Use TCC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

A	D						
X	X						

2.21.2 Dithering Mode with External Retrigger Events

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or shrink of left-aligned pulses.

Workaround
Do not use retrigger events or actions when the TCC module is configured in Dithering mode.

Affected Silicon Revisions

A	D						
X	X						

2.21.3 ALOCK Feature

ALOCK feature is not functional.

Workaround

None.

Affected Silicon Revisions

A	D						
X	X						

2.21.4 LUPD feature in Down-Counting Mode

In down-counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.

Workaround

None.

Affected Silicon Revisions

A	D						
X	X						

2.22 Position Decoder (PDEC)

2.22.1 Reserved

2.23 Voltage Reference System

2.23.1 Temperature Sensor

Both internal temperature sensors, TSENSP and TSENSC, are not supported and should not be used.

Workaround

None.

Affected Silicon Revisions

A	D						
X	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the device data sheet (DS60001507**F**), and are showed in **BOLD** type:

There are currently no Data Sheet Clarifications to report.

4. Appendix A: Revision History

Rev. K (05/2020)
The following Silicon Errata was removed as the issue does not exist:

- 2.22.1 X2 Mode

The following silicon errata were updated:

- 2.6.6 Device Operation for Temperature < -20℃ was updated with a table denoting those packages affected by the issue

The following silicon errata was added:

- 2.18.19 USART

Obsolete Data Sheet Clarifications were removed.

Rev. J (11/2019)
Added new silicon errata for 2.23.1 Voltage Reference System.

Rev. H (7/2019)
The Silicon errata for Device Operation for Temperature < -20°C was updated with text denoting which silicon versions it applies to.

Rev. G (6/2019)
The Errata Summary Table and The affected silicon revision tables in 2. Silicon Errata Issues have been updated to reflect the addition of EFP and Non-EFP silicon revisions.
The following Silicon issues were added:

- ADC:
  - 2.1.4 DMA Sequencing
  - 2.1.5 DMA Sequencing
- AC: 2.2.2 Output
- DFLL48: 2.8.4 LLAW
- DAC: 2.9.5 Reference
- RTC: 2.17.6 Prescaler
- SERCOM:
  - 2.18.17 Wakeup
  - 2.18.18 LENGTH

Rev F. (2/2019)
The following Silicon Issues were updated:

- FDPLL: Low-Frequency Input Clock on FDPLLn

The following Data Sheet Clarifications were added:

- Update to Initialization, Enabling, Disabling, and Resetting
- Update to Loop Divider Ratio Updates

Rev. E (11/2018)
The following silicon issues were added:

- SERCOM I^2C
  - 2.18.16 SERCOM I2C: Repeated Start
- CAN-FD
  - 2.4.3 Message Transmitted with Wrong Arbitration and Control Fields

  - 2.4.4 DAR Mode
  - 2.4.5 High-Priority Message (HPM) interrupt
  - 2.4.6 Tx FIFO message sequence inversion
- DMAC
  - 2.10.2 Channel Priority
  - 2.10.3 DMAC in Debug Mode
- RTC
  - 2.17.2 COUNTSYNC
  - 2.17.3 Tamper Input Filter
  - 2.17.4 Tamper Detection
  - 2.17.5 Tamper Detection Timestamp
- SUPC
  - BOD33 Hysteresis
- TCC
  - 2.21.3 ALOCK Feature
  - 2.21.4 LUPD feature in Down-Counting Mode

The following Data Sheet Clarifications were added:

- Table 54-35 Flash Timing Characteristics was updated.
- BOD12 Register Information was updated.

Rev. D (08/2018)
The current device data sheet revision letter was updated.

The following silicon issues were added:

- Configurable Custom Logic (CCL):
  - Enable Protected Registers
  - Sequential Logic Reference
- Device:
  - Reverse Current in VDDIOB Domain
- SERCOM:
  - Repeated Start in High-Speed Master Write Operation
  - Repeated Start in High-Speed Master Read Operation
  - STATUS.CLKHOLD Bit in Master and Slave Modes
- Supply Controller (SUPC):
  - Buck Converter Mode
- TCC:
  - TCC with EVSYS in SYNC/RESYNC Mode

Rev. C (04/2018)
The current device data sheet revision letter was updated.

The following silicon issues were added:

- Analog-to-Digital Converter (ADC):
  - Reference Buffer Offset Compensation
- Peripheral Access Controller (PAC):
  - PAC Protection
  - PAC Protection
- Real-Time Counter (RTC):
  - Write Corruption
- SERCOM-I2C:
  - Slave Mode with DMA

  - I^2C Slave in DATA32B Mode
  - I^2C Slave Mode in 10-bit Address
  - Repeated Start
- SERCOM-SPI
  - Data Preload
- SERCOM-UART:
  - Collision Detection

All Data Sheet Clarifications were removed.

Rev. B (10/2017)
This revision includes the following additions:

Silicon Issues
- Ethernet Functionality in 64-pin Packages

Data Sheet Clarifications
- ADC Operating Conditions
- GMAC IEEE 802.3AZ Energy Efficient Support
- SERCOM Baud Rate Equations
- SERCOM in SPI Mode Timing
- TQFP 64-pin Package
- DAC Operating Conditions

Rev. A (7/2017)
Initial release of this document.

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