# Ultra Low Dropout 1A, 2A, 3A Low Input Voltage NMOS LDOs

## ISL80111, ISL80112, ISL80113

The ISL80111, ISL80112, and ISL80113 are ultra low dropout LDOs providing the optimum balance between performance, size and power consumption in size constrained designs for data communication, computing, storage and medical applications. These LDOs are specified for 1A, 2A and 3A of output current and are optimized for low voltage conversions.Operating with a $V_{IN}$ of 1V to 3.6V and with a legacy 3.3V to 5V on the BIAS, the $V_{OUT}$ is adjustable from 0.8V to 3.3V. With a $V_{IN}$ PSRR greater than 40dB at 100kHz makes these LDOs an ideal choice in noise sensitive applications. The guaranteed ±1.6% $V_{OUT}$ accuracy overall conditions lends these parts to suppling an accurate voltage to the latest low voltage digital ICs.

An enable input allows the part to be placed into a low quiescent current shutdown mode. A submicron CMOS process is utilized for this product family to deliver best-in-class analog performance and overall value for applications in need of input voltage conversions typically below 2.5V. It also has the superior load transient regulation unique to a NMOS power stage. These LDOs consume significantly lower quiescent current as a function of load compared to bipolar LDOs.

## Features

- Ultra low dropout: 75mV at 3A, (typ)
- Excellent $V_{IN}$ PSRR: 70dB at 1kHz (typ)
- ±1.6% guaranteed $V_{OUT}$ accuracy for -40°C < $T_J$ < +125°C
- Very fast load transient response
- Extensive protection and reporting features
- $V_{IN}$ range: 1V to 3.6V, $V_{OUT}$ range: 0.8V to 3.3V
- Small 10 Ld 3x3 DFN package

## Applications

- Noise-sensitive instrumentation and medical systems
- Data acquisition and data communication systems
- Storage, telecommunications and server equipment
- Low voltage DSP, FPGA and ASIC core power supplies
- Post-regulation of switched mode power supplies

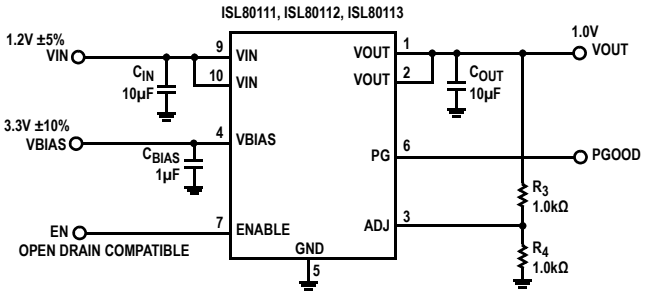



FIGURE 1. TYPICAL APPLICATION SCHEMATIC

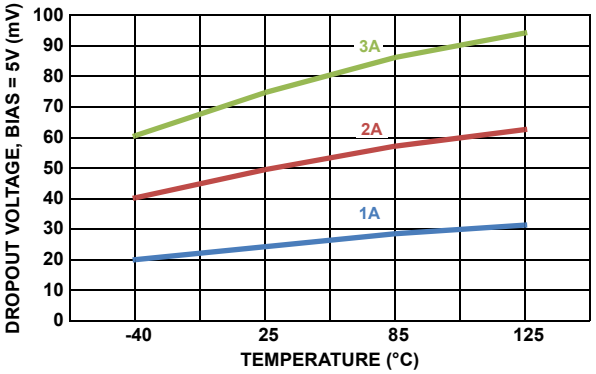



FIGURE 2. DROPOUT VOLTAGE OVER-TEMP AND $I_{OUT}$

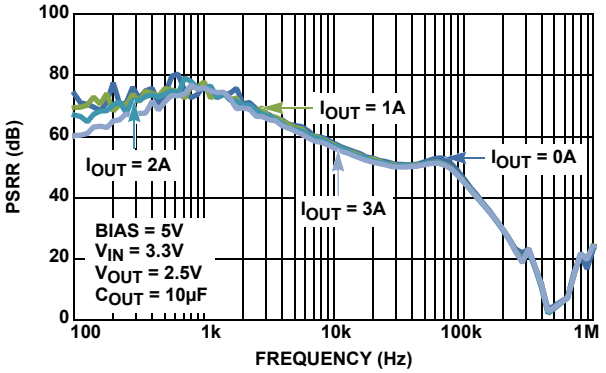



FIGURE 3. $V_{IN}$ PSRR vs LOAD CURRENT (ISL80113)

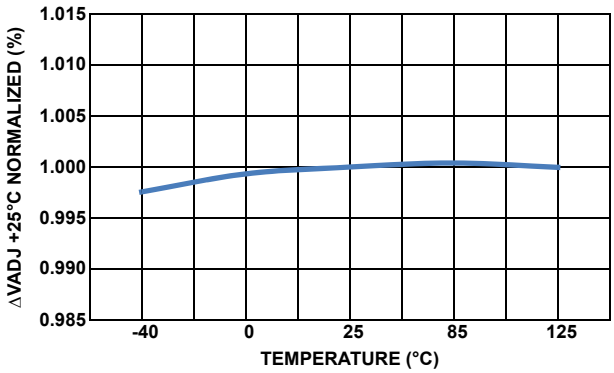
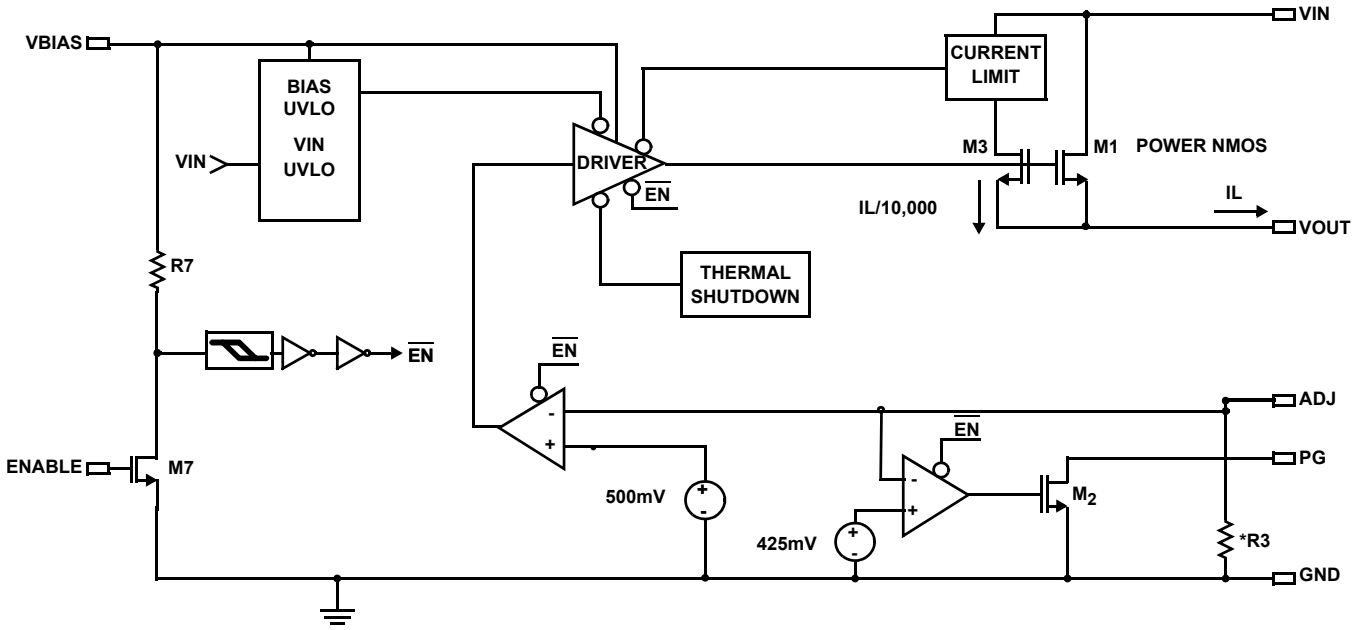


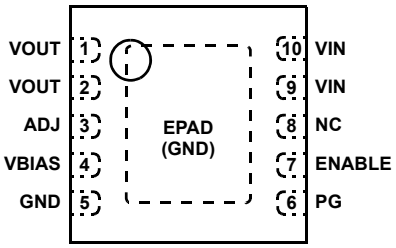

FIGURE 4. $\Delta V_{ADJ}$ vs TEMPERATURE

## Block Diagram




## Pin Configuration

ISL80111, ISL80112, ISL80113
(10 LD 3X3 DFN)
TOP VIEW




## Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1, 2 | VOUT | Output voltage pin. Range 0.8V to 3.3V |
| 3 | ADJ | ADJ pin for externally setting $V_{OUT}$. Range 0.5V to $V_{OUT}$ |
| 4 | VBIAS | Bias voltage pin for internal control circuits. Range 2.9V to 5.5V |
| 5 | GND | Ground pin |
| 6 | PG | $V_{OUT}$ in regulation signal. Logic low defines when $V_{OUT}$ is not in regulation. Range 0V to BIAS |
| 7 | ENABLE | $V_{IN}$ independent chip enable. TTL and CMOS compatible. Range 0V to $V_{BIAS}$ |
| 8 | NC | No Connect |
| 9, 10 | VIN | Input supply pins. Range 1.0V to 3.6V |
| | EPAD | EPAD at ground potential. It is recommended to solder the EPAD to the ground plane. |

# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | $V_{OUT}$ (V) | TEMP RANGE (°C) | PACKAGE (Pb-Free) | PKG DWG. # |
|---|---|---|---|---|---|
| ISL80111IRAJZ | 1ADJ | ADJ | -40 to +85 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80112IRAJZ | 2ADJ | ADJ | -40 to +85 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80113IRAJZ | 3ADJ | ADJ | -40 to +85 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80111EVAL1Z | ISL80111 Evaluation Board | | | | |
| ISL80112EVAL1Z | ISL80112 Evaluation Board | | | | |
| ISL80113EVAL1Z | ISL80113 Evaluation Board | | | | |

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information pages for ISL80111, ISL80112, and ISL80113. For more information on MSL please see Tech Brief TB363.

## Absolute Maximum Ratings (Note4)

$V_{IN}$ Relative to GND ..... -0.3 to +6V
$V_{OUT}$ Relative to GND ..... -0.3 to +4V
PG, ENABLE, SENSE/ADJ, Relative to GND (Note 5) ..... -0.3 to +6V
$V_{BIAS}$ Relative to GND ..... -0.3V to +6V
PG Rated Current (Note 6) ..... 10mA
ESD Rating
Human Body Model (Tested per JESD22-A114E) ..... 4000V
Machine Model (Tested per JESD22-115-A) ..... 300V
Charged Device Model ..... 2000V
Latch Up ..... 100mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 10 Ld 3x3 DFN Package (Notes 7, 8) ..... | 48 | 4 |

Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile ..... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions (Notes 4, 6)

Junction Temperature Range ..... -40°C to +125°C
$V_{IN}$ Relative to GND (ISL80113) (Note 9) ..... $V_{OUT}$ + 0.4V to 5V
$V_{IN}$ Relative to GND (ISL80112) (Note 9) ..... $V_{OUT}$ + 0.3V to 5V
$V_{IN}$ Relative to GND (ISL80111) (Note 9) ..... $V_{OUT}$ + 0.2V to 5V
Nominal $V_{OUT}$ Range ..... 800mV to 3.3V
PG, ENABLE, SENSE/ADJ, SS Relative to GND ..... 0V to 5.5V
$V_{BIAS}$ Relative to GND ..... 0V to 5.5V
$V_{BIAS}$ Relative to $V_{OUT}$ ..... +0.8V minimum

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. Absolute maximum ratings define limits of safe operation. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
5. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
6. Electromigration specification defined as lifetime average junction temperature of +110°C where maximum rated DC current = lifetime average current.
7. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.
9. Minimum operating voltage applied to $V_{IN}$ is 1V if $V_{IN}$ - $V_{DO}$ < 1V

## Electrical Specifications

Unless otherwise specified, $V_{IN}$ = $V_{OUT}$ + 0.4V, $V_{BIAS}$ = 2.9V, $V_{OUT}$ = 1.2V, $C_{BIAS}$ = 1µF, $C_{IN}$ = 10µF, $C_{OUT}$ = 2.2µF, $T_J$ = +25°C, $I_L$ = 0mA. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to “Power Dissipation” on page 13 and Tech Brief TB379.
**Boldface limits apply over junction temperature ($T_J$) range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J$ = $T_A$ where datasheet limits are defined.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $V_{BIAS}$ UVLO | UVLO_BIAS_r | $V_{BIAS}$ Rising | | 2.3 | **2.9** | V |
| | UVLO_BIAS_f | $V_{BIAS}$ Falling | **1.55** | 2.1 | **2.8** | V |
| $V_{BIAS}$ UVLO Hysteresis | $UVLO_{B\_HYS}$ | | | 0.2 | | V |
| DC ADJ Pin Voltage Accuracy | $V_{ADJ}$ | 1.0V ≤ $V_{IN}$ ≤ 3.6V, $I_{LOAD}$ = 0A, 2.9V ≤ $V_{BIAS}$ ≤ 5.5V, $V_{OUT}$ = $V_{ADJ}$ | **494** | 502 | **510** | mV |
| DC Input Line Regulation | $\Delta V_{OUT}$ | $V_{OUT}$ + 0.4V ≤ $V_{IN}$ ≤ 3.6V | | 0.01 | **0.9** | mV |
| DC Bias Line Regulation | $\Delta V_{OUT}$ | 2.9V<$V_{BIAS}$<5.5V with respect to ADJ pin | | 0.3 | **1.4** | mV |
| DC Output Load Regulation | $\Delta V_{OUT}$ | 0A ≤ $I_{LOAD}$ ≤ 3A | **-2** | -0.2 | **2** | mV |
| Feedback Input Current | | $V_{ADJ}$ = 0.5V | | 10 | **80** | nA |
| $V_{IN}$ Quiescent Current | $I_Q$ ($V_{IN}$) | VOUT = 2.5V | | 8 | **10** | mA |
| $V_{IN}$ Quiescent Current | $I_Q$ ($V_{IN}$) | VOUT = 3.3, | | 10.6 | | mA |

## Electrical Specifications

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{BIAS} = 2.9V$, $V_{OUT} = 1.2V$, $C_{BIAS} = 1\mu F$, $C_{IN} = 10\mu F$, $C_{OUT} = 2.2\mu F$, $T_J = +25°C$, $I_L = 0mA$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Power Dissipation" on page 13 and Tech Brief TB379.

**Boldface limits apply over junction temperature ($T_J$) range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ where datasheet limits are defined. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|---|---|---|---|---|---|---|
| $V_{IN}$ Quiescent Current | $I_Q$ ($V_{IN}$) | VOUT = 1.0V | | 3.5 | | mA |
| $V_{BIAS}$ Quiescent Current | $I_Q$ ($V_{BIAS}$) | $0 \le I_L \le 3A$, $V_{BIAS} = 5.5V$ | | 2.9 | **4.6** | mA |
| Ground Pin Current in Shutdown | $I_{SHDN}$ | ENABLE Pin = 0.2V, $T_J = +125°C$ | | 3 | **20** | µA |
| $V_{IN}$ Dropout Voltage (Note 11) | $V_{DO(VIN)}$ | $I_{LOAD} = 1A$, $V_{OUT} = 1.2V$, $2.9V \le V_{BIAS} \le 5V$ | | 27 | **90** | mV |
| | | $I_{LOAD} = 2A$, $V_{OUT} = 1.2V$, $2.9V \le V_{BIAS} \le 5V$ | | 53 | **115** | mV |
| | | $I_{LOAD} = 3A$, $V_{OUT} = 1.2V$, $2.9V \le V_{BIAS} \le 5V$ | | 75 | **140** | mV |
| $V_{BIAS}$ Dropout Voltage (Note 11) | $V_{DO(BIAS)}$ | $I_{LOAD} = 1A$, $V_{OUT} = 1.2V$ | | 1.1 | **1.3** | V |
| | | $I_{LOAD} = 2A$, $V_{OUT} = 1.2V$ | | 1.2 | **1.4** | V |
| | | $I_{LOAD} = 3A$, $V_{OUT} = 1.2V$ | | 1.3 | **1.5** | V |
| **OVERCURRENT PROTECTION** | | | | | | |
| Output Short Circuit Current (3A Version) | ISC | $V_{OUT} = 0.2V$ | | 5.2 | | A |
| Output Short Circuit Current (2A Version) | | $V_{OUT} = 0.2V$ | | 3.2 | | A |
| Output Short Circuit Current (1A Version) | | $V_{OUT} = 0.2V$ | | 2.2 | | A |
| **OVER-TEMPERATURE PROTECTION** | | | | | | |
| Thermal Shutdown Temperature | TSD | | | 160 | | °C |
| Thermal Shutdown Hysteresis | TSDn | | | 20 | | °C |
| **AC CHARACTERISTICS** | | | | | | |
| Input Supply Ripple Rejection | PSRR($V_{IN}$) | f = 120Hz, $I_{LOAD} = 1A$ | | 80 | | dB |
| | PSRR($V_{BIAS}$) | f = 120Hz, $I_{LOAD} = 1A$ | | 60 | | dB |
| Output Noise Voltage | $e_{N(RMS)}$ | $I_{LOAD} = 10mA$, BW = 100Hz ≤ f ≤ 100kHz | | 100 | | $\mu V_{RMS}$ |
| Spectral Noise Density | $e_N$ | $I_{LOAD} = 3A$, f = 10Hz | | 7 | | $\mu V/\sqrt{Hz}$ |
| | | $I_{LOAD} = 3A$, f = 100Hz | | 3 | | $\mu V/\sqrt{Hz}$ |
| DEVICE START-UP CHARACTERISTICS | | | | | | |
| EN Start-up Time | $t_{EN}$ | $C_{OUT} = 10\mu F$, $I_{LOAD} = 1A$ | | 50 | | µs |
| BIAS Start-up Time | $t_{BIAS}$ | $C_{OUT} = 10\mu F$, EN = BIAS | | 100 | | µs |
| **ENABLE PIN CHARACTERISTICS** | | | | | | |
| Turn-on Threshold (Rising) | | $V_{OUT} + 0.4V \le V_{IN} \le 3.6V$, $2.9V \le V_{BIAS} \le 5.5V$ | **400** | 680 | **850** | mV |
| Hysteresis (Rising Threshold) | | $1.2V \le V_{IN} \le 3.6V$, $2.9V \le V_{BIAS} \le 5.5V$ | **60** | 260 | **330** | mV |
| **PG PIN CHARACTERISTICS** | | | | | | |
| PG Flag Falling Threshold | $PG_{TH}$ | $2.9V \le V_{BIAS} \le 5.5V$ | **71** | 82 | **93** | $\%V_{OUT}$ |
| PG Flag Hysteresis | PGHYS | $2.9V \le V_{BIAS} \le 5.5V$ | | 9.3 | | $\%V_{OUT}$ |

**Electrical Specifications** Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{BIAS} = 2.9V$, $V_{OUT} = 1.2V$, $C_{BIAS} = 1\mu F$, $C_{IN} = 10\mu F$, $C_{OUT} = 2.2\mu F$, $T_J = +25°C$, $I_L = 0mA$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. Please refer to "Power Dissipation" on page 13 and Tech Brief TB379.

**Boldface limits apply over junction temperature ($T_J$) range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ where datasheet limits are defined. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|---|---|---|---|---|---|---|
| PG Flag Low Voltage | | $I_{SINK}$ = 500µA | | 90 | **130** | mV |
| PG Flag Leakage Current | | PG = $V_{BIAS}$ = 5.5V | | 11 | **300** | nA |
| PG Flag Sink Current | | | **7** | 10 | | mA |

NOTES:

10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
11. Dropout is defined by the difference in supply ($V_{IN}$, $V_{BIAS}$) and $V_{OUT}$ when the supply produces a 2% drop in $V_{OUT}$ from its nominal value, output voltage set to 2.5V.
12. For normal operation, $V_{IN}$ must always be less than or equal to the voltage applied to $V_{BIAS}$. Part is protected against fault conditions where $V_{IN}$ can be greater than $V_{BIAS}$.

## Typical Operating Performance

Unless otherwise noted, $V_{IN}$ = 1.8V, $V_{BIAS}$ = 3.3V, $V_{OUT}$ = 1.2V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_{LOAD}$ = 0A.

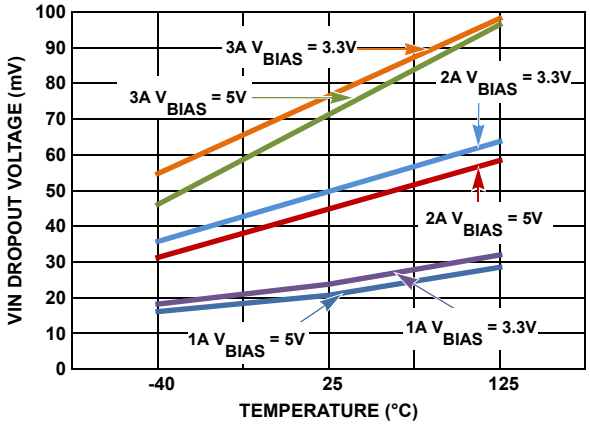



FIGURE 5. DROPOUT vs $V_{BIAS}$

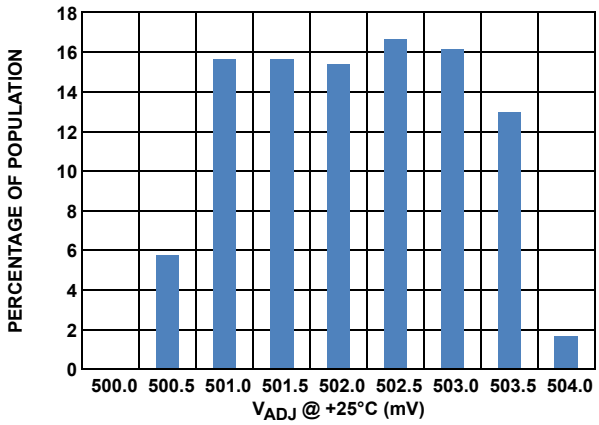



FIGURE 6. $V_{ADJ}$ DISTRIBUTION

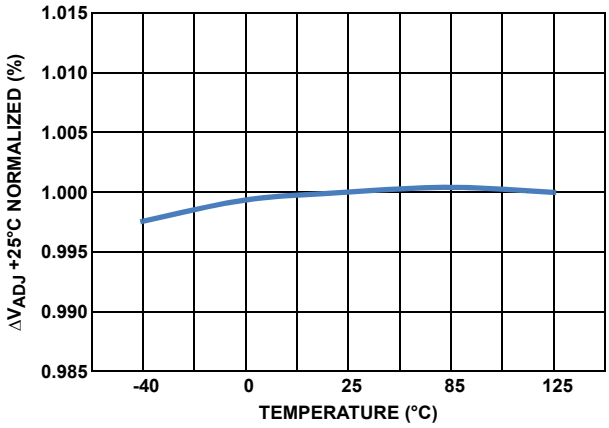



FIGURE 7. $\Delta V_{ADJ}$ vs TEMPERATURE

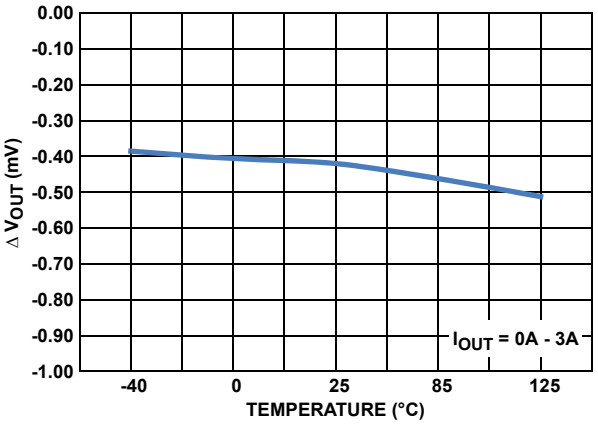



FIGURE 8. LOAD REGULATION vs TEMPERATURE

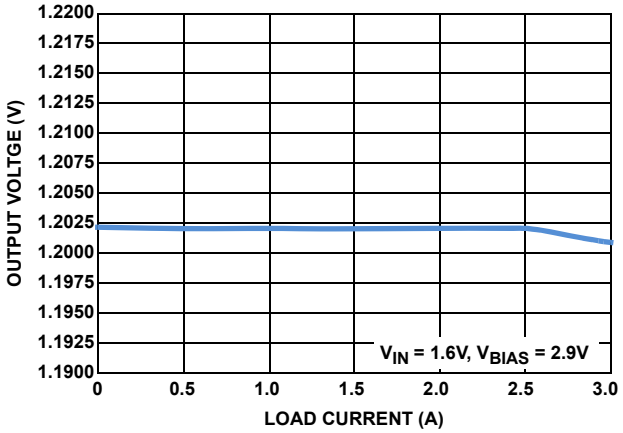



FIGURE 9. LOAD REGULATION, $V_{OUT}$ vs $I_{OUT}$

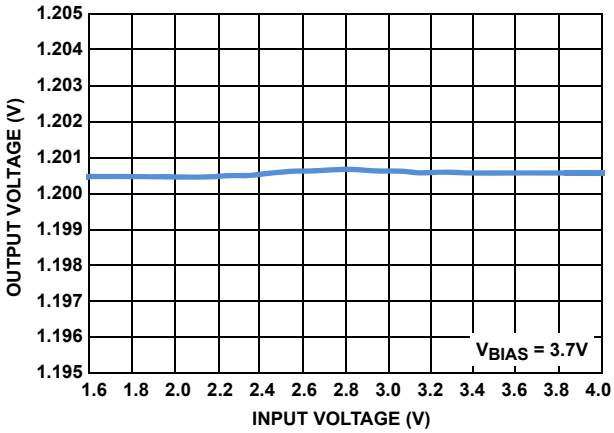



FIGURE 10. $V_{IN}$ LINE REGULATION

## Typical Operating Performance

Unless otherwise noted, $V_{IN}$ = 1.8V, $V_{BIAS}$ = 3.3V, $V_{OUT}$ = 1.2V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_{LOAD}$ = 0A. **(Continued)**

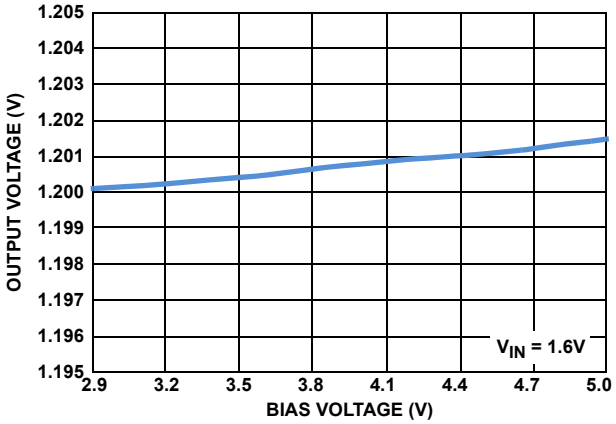



FIGURE 11. $V_{BIAS}$ LINE REGULATION

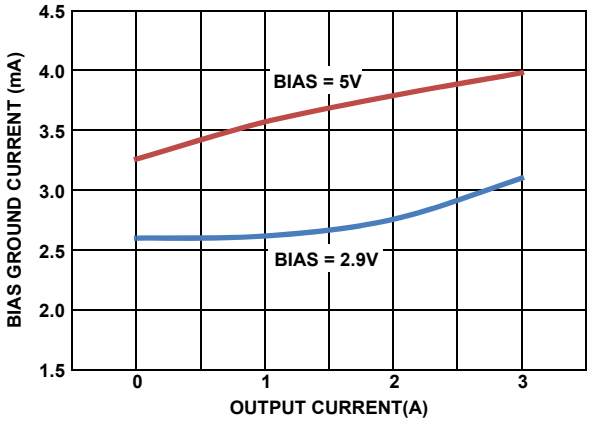



FIGURE 12. BIAS GROUND CURRENT vs LOAD CURRENT

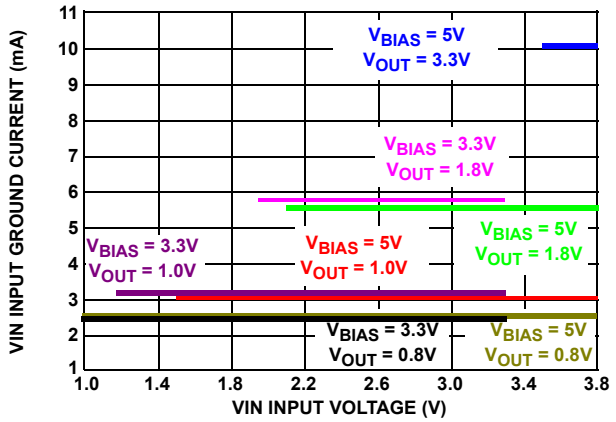



FIGURE 13. INPUT GROUND CURRENT vs $V_{IN}$ and $V_{OUT}$

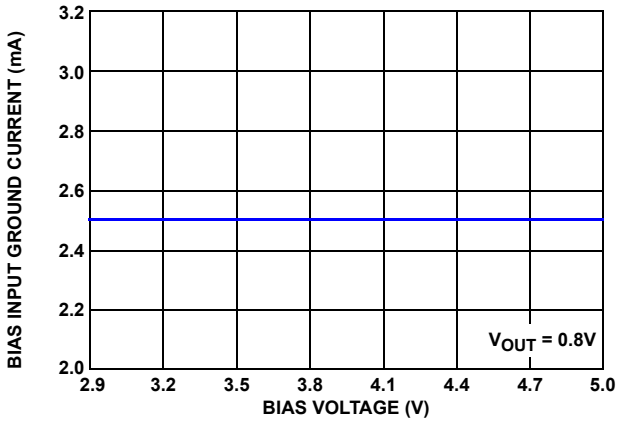



FIGURE 14. INPUT GROUND CURRENT vs $V_{BIAS}$

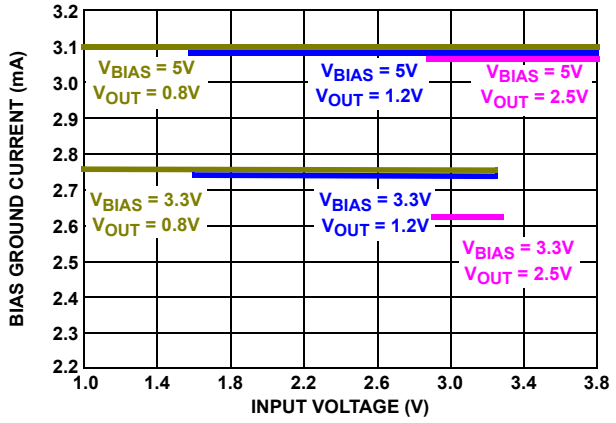



FIGURE 15. BIAS GROUND CURRENT vs $V_{IN}$ and $V_{OUT}$

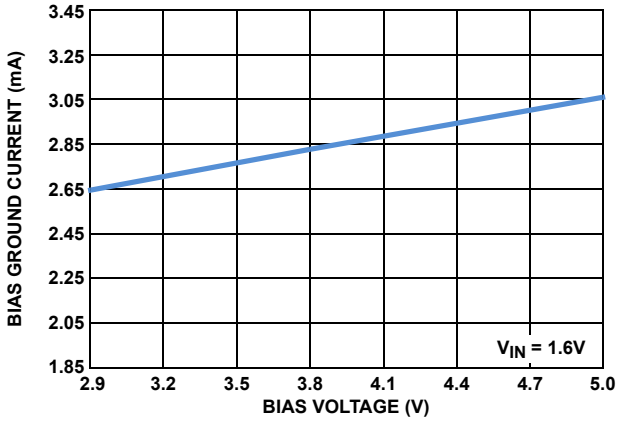



FIGURE 16. BIAS GROUND CURRENT vs $V_{BIAS}$

## Typical Operating Performance

Unless otherwise noted, $V_{IN}$ = 1.8V, $V_{BIAS}$ = 3.3V, $V_{OUT}$ = 1.2V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_{LOAD}$ = 0A. **(Continued)**

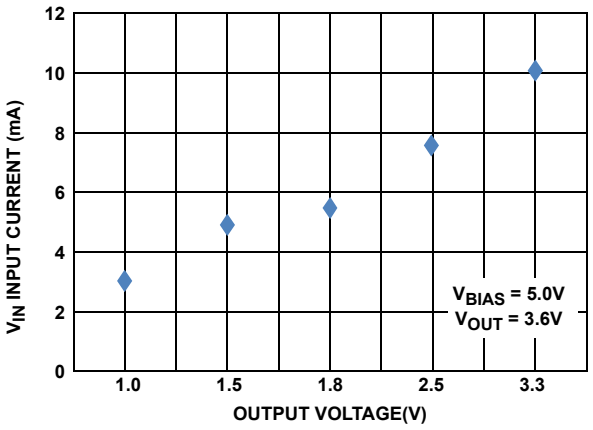



FIGURE 17. $V_{IN}$ $I_Q$ vs VOUT VOLTAGE

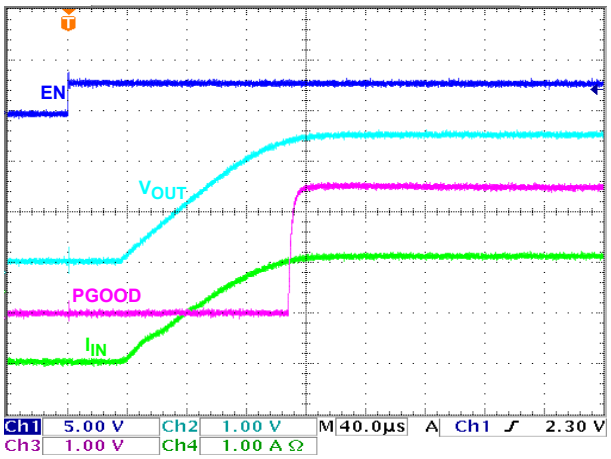



FIGURE 18. ENABLE START-UP WITH PGOOD

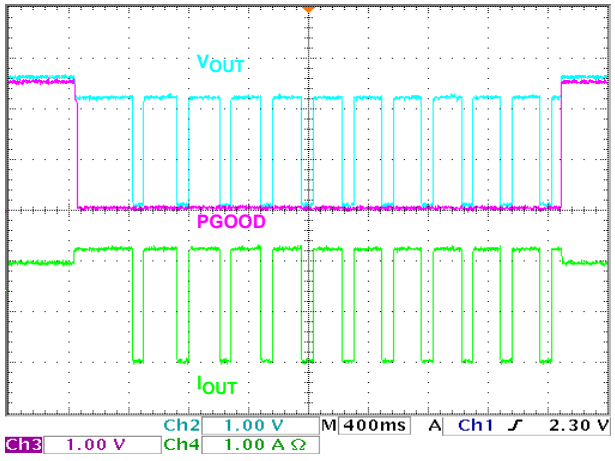



FIGURE 19. ISL8011X INTO AND OUT OF THERMAL SHUTDOWN

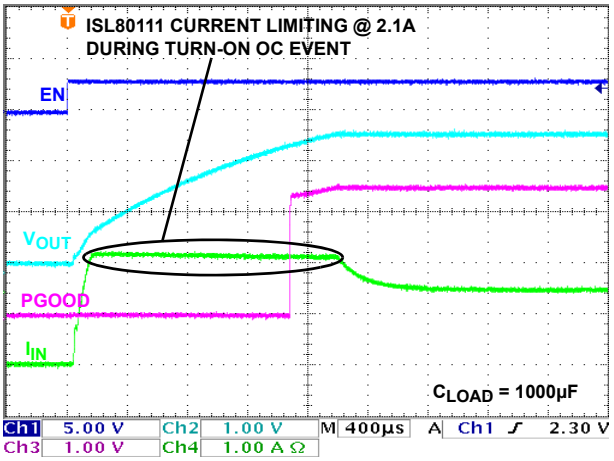



FIGURE 20. ISL80111 ENABLED INTO OVERCURRENT

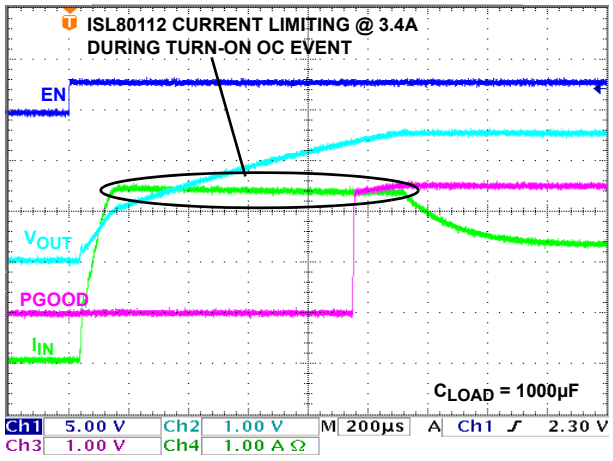



FIGURE 21. ISL80112 ENABLED INTO OVERCURRENT

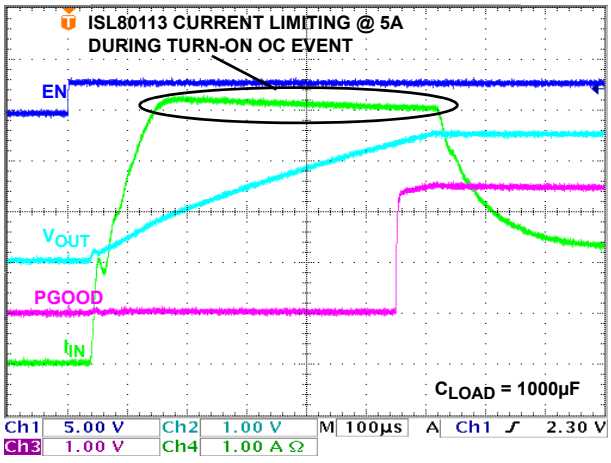



FIGURE 22. ISL80113 ENABLED INTO OVERCURRENT

## Typical Operating Performance

Unless otherwise noted, $V_{IN}$ = 1.8V, $V_{BIAS}$ = 3.3V, $V_{OUT}$ = 1.2V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_{LOAD}$ = 0A. **(Continued)**

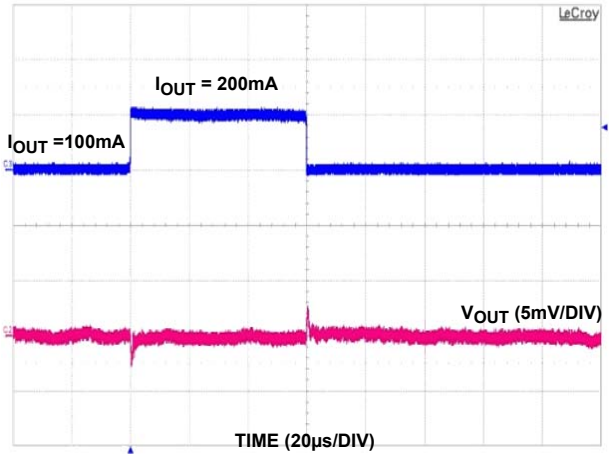



FIGURE 23. 100mA LOAD TRANSIENT RESPONSE

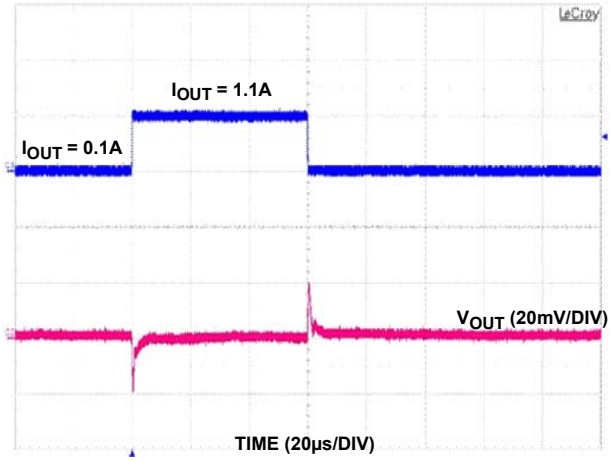



FIGURE 24. 1A LOAD TRANSIENT RESPONSE

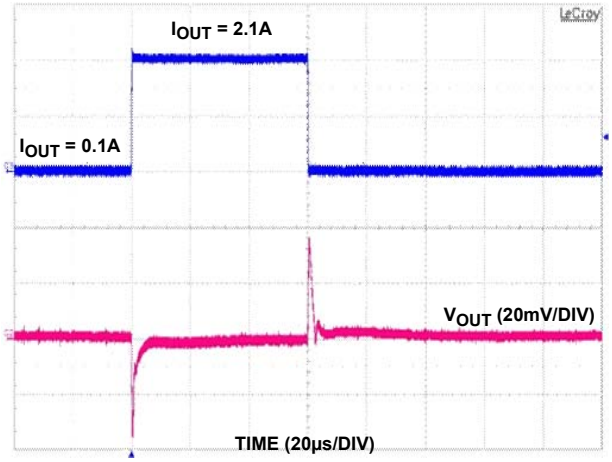



FIGURE 25. 2A LOAD TRANSIENT RESPONSE

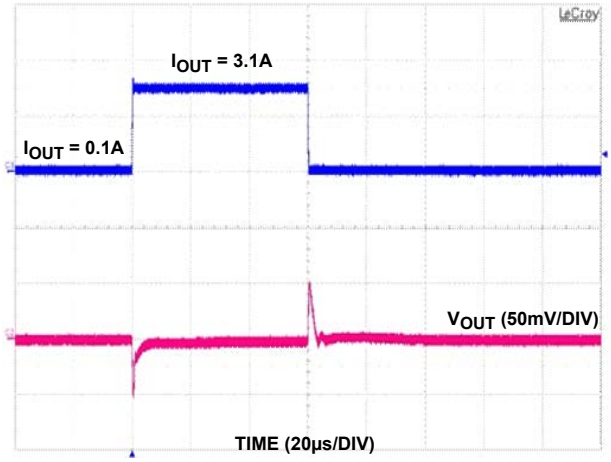



FIGURE 26. 3A LOAD TRANSIENT RESPONSE

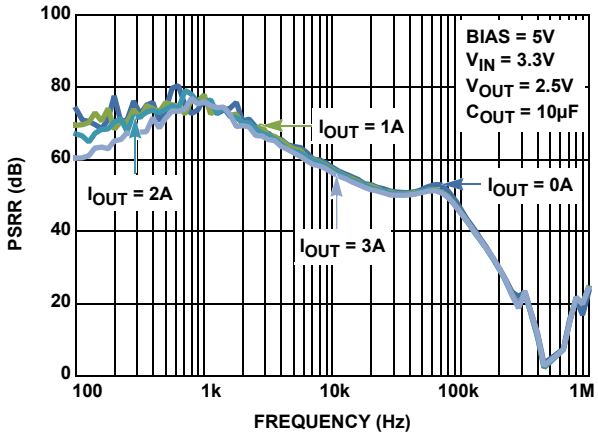



FIGURE 27. $V_{IN}$ PSRR vs LOAD CURRENT

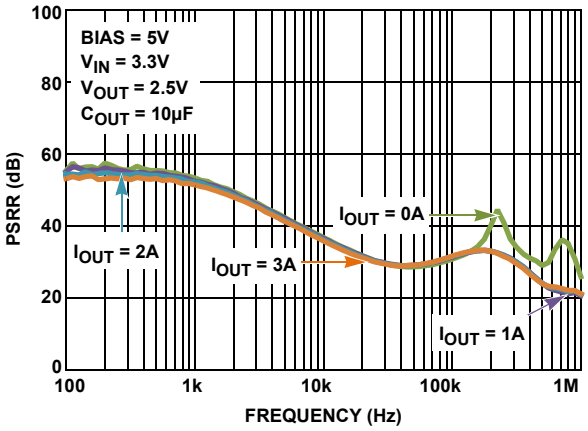



FIGURE 28. BIAS PSRR vs LOAD CURRENT

## Typical Operating Performance

Unless otherwise noted, $V_{IN}$ = 1.8V, $V_{BIAS}$ = 3.3V, $V_{OUT}$ = 1.2V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_{LOAD}$ = 0A. **(Continued)**

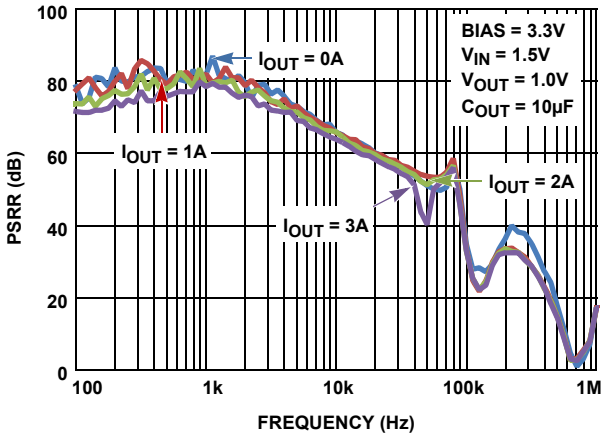



FIGURE 29. $V_{VIN}$ PSRR vs LOAD CURRENT

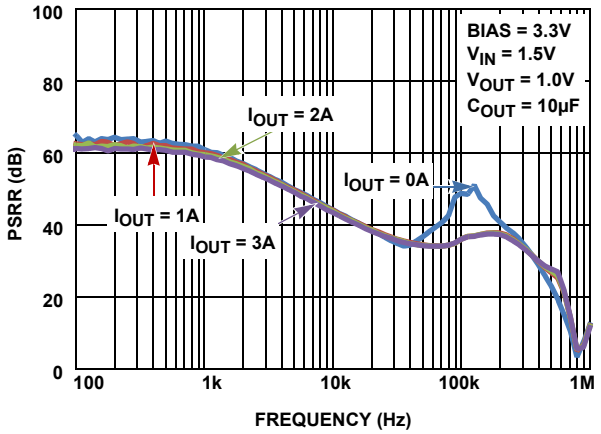



FIGURE 30. $V_{BIAS}$ PSRR vs LOAD CURRENT

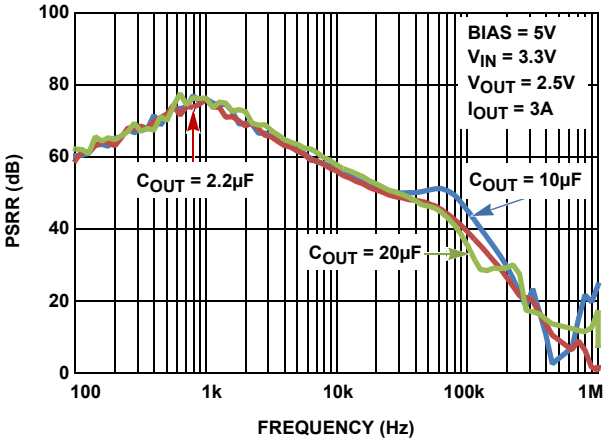



FIGURE 31. $V_{IN}$ PSRR vs $C_{OUT}$

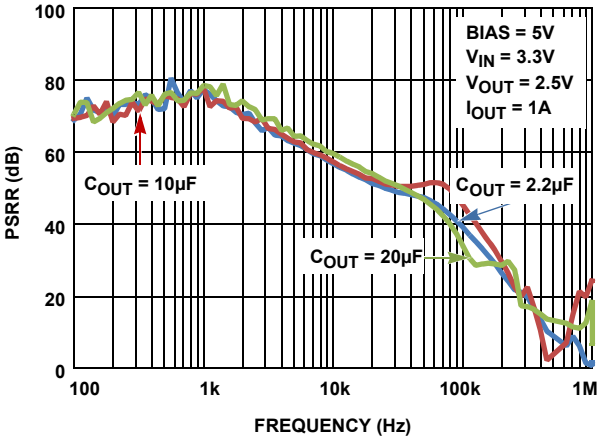



FIGURE 32. $V_{IN}$ PSRR vs $C_{OUT}$

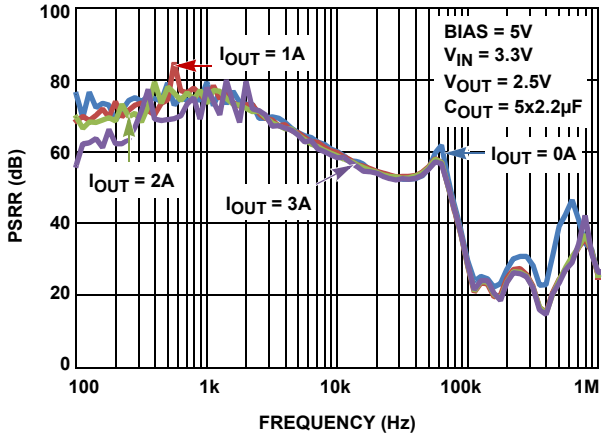



FIGURE 33. $V_{IN}$ PSRR vs LOAD CURRENT

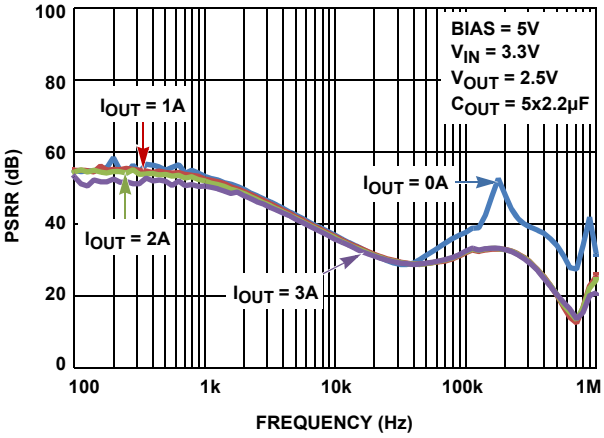



FIGURE 34. $V_{BIAS}$ PSRR vs LOAD CURRENT

## Typical Operating Performance

Unless otherwise noted, $V_{IN}$ = 1.8V, $V_{BIAS}$ = 3.3V, $V_{OUT}$ = 1.2V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_{LOAD}$ = 0A. **(Continued)**

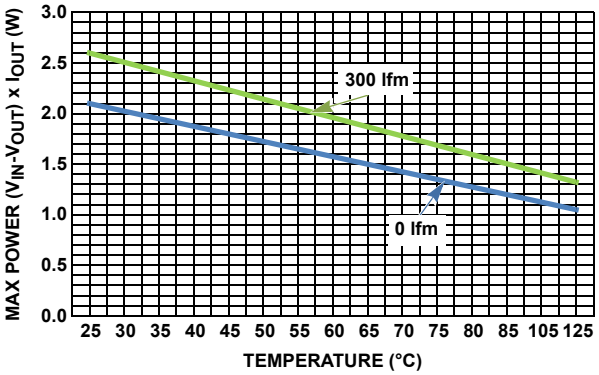



FIGURE 35. CONTINUOUS POWER LIMIT vs AIR TEMP AND FLOW

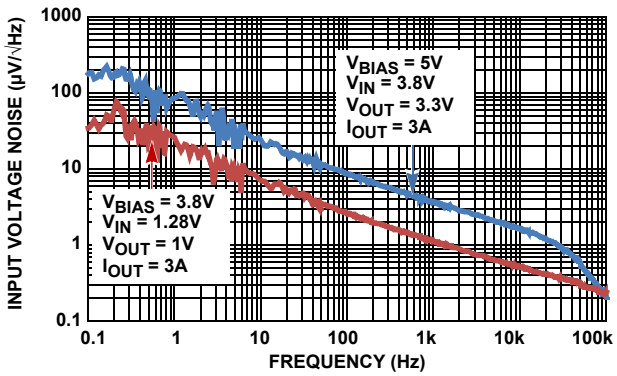



FIGURE 36. INPUT VOLTAGE NOISE vs BIAS VOLTAGE

# Functional Description

The ISL80111, ISL80112 and ISL80113 are high-performance, low-dropout regulators featuring an NMOS pass device. Benefits of using an NMOS as a pass device include low input voltage, stability over a wide range of output capacitors, and ultra low dropout voltage. The ISL80111, ISL80112 and ISL80113 are ideal for post regulation of switch mode power supplies.

The ISL80111, ISL80112 and ISL80113 also integrate enable, power-good indicator, current limit protection, and thermal shutdown functions into a space-saving 3x3 DFN package.

## Input Voltage Requirements

The VIN pin provides the high current to the drain of the NMOS pass transistor. The specified minimum input voltage is 1V and dropout voltage for this family of LDOs has been conservatively specified.

## Bias Voltage Requirements

The $V_{BIAS}$ input powers the internal control circuits, reference voltage, and LDO gate driver. The difference between the $V_{BIAS}$ voltage and the output voltage must be greater than the $V_{BIAS}$ dropout voltage specified in the "Electrical Specifications" table beginning on Page 4. The minimum $V_{BIAS}$ input is 2.9V.

## Enable Operation

The ENABLE turn-on threshold is typically 600mV with a hysteresis of 100mV. This pin must not be left floating. When this pin is not used, it must be tied to $V_{BIAS}$. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the ENABLE pin.

## Soft-start Operation

The ISL8011x has an internal 100µs typical soft-start function to prevent excessive in-rush current during start-up.

## Power-good Operation

The PGOOD flag is an open-drain NMOS that can sink up to 10mA during a fault condition. Applications not using this feature must connect this pin to ground. The PGOOD pin requires an external pull-up resistor, which is typically connected to the $V_{OUT}$ pin. The PGOOD pin should not be pulled up to a voltage source greater than $V_{BIAS}$. A PGOOD fault can be caused by the output voltage going below 84% of the nominal output voltage. PGOOD does not function during thermal shutdown as the $V_{OUT}$ is less than the minimum regulation voltage during that time.

## Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 4V. Referring to Figure 1 the external resistor divider, $R_3$ and $R_4$, is used to set the output voltage as shown in Equation 1. The recommended value for $R_4$ is 500Ω to 1kΩ. $R_3$ is then chosen according to Equation 2.

$$V_{OUT} = 0.5V \times \left(\frac{R_3}{R_4} + 1\right) \quad \text{(EQ. 1)}$$

$$R_3 = R_4 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 2)}$$

## Current Limit Protection

The ISL80111, ISL80112, and ISL80113 incorporate protection against overcurrent due to a short, overload condition applied to the output and the in-rush current that occurs at start-up. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in "Electrical Specifications" on page 4. If the short or overload condition is removed from $V_{OUT}$, then the output returns to normal voltage mode regulation. In the event of an overload condition, the LDO might begin to cycle on and off due to the die temperature exceeding the thermal fault condition.

## Thermal Fault Protection

If the die temperature exceeds (typically) +160°C, the LDO output shuts down until the die temperature cools to (typically) +140°C. The level of power, combined with the thermal impedance of the package (+48°C/W), determines whether the junction temperature exceeds the thermal shutdown temperature.

See Figure 35 for maximum continuous power dissipation guidance for ambient temperature and linear air flow rate. This graph ignores the insignificant power dissipation contribution of the BIAS pin.

# External Capacitor Requirements

External capacitors are required for proper operation. To ensure optimal performance, careful attention must be paid to the layout guidelines and selection of capacitor type and value.

## Input Capacitor

The minimum input capacitor required for proper operation is 10µF with a ceramic dielectric. This minimum capacitor must be connected to the $V_{IN}$ and ground pins of the LDO no further than 0.5cm away.

## Output Capacitor

The ISL8011x applies state-of-the-art internal compensation to simplify selection of the output capacitor. Stable operation over the full temperature range, $V_{IN}$ range, $V_{OUT}$ range, and load extremes is guaranteed for all capacitor types and values, assuming a 1µF X5R/X7R is used for local bypass on $V_{OUT}$. This minimum capacitor must be connected to the $V_{OUT}$ and ground pins of the LDO no further than 0.5cm away.

Lower-cost Y5V and Z5U type ceramic capacitors are acceptable, if the size of the capacitor is larger, to compensate for the significantly lower tolerance over X5R/X7R types. Additional capacitors of any value, in ceramic, POSCAP, or alum/tantalum electrolytic types, can be placed in parallel to improve PSRR at higher frequencies or load-transient AC output voltage tolerances.

## Bias Capacitor

The minimum input capacitor required for proper operation is 1µF with a ceramic dielectric. This minimum capacitor must be connected to the $V_{BIAS}$ and ground pins of the LDO no further than 0.5cm away. When the VBIAS pin is connected to the $V_{IN}$ pin, a total of 10µF of X5R/X7R connected to the $V_{IN}$ pin and ground is sufficient.

# Power Dissipation and Thermals

## Power Dissipation

Junction temperature must not exceed the range specified in the “Recommended Operating Conditions” section on Page 4. Power dissipation can be calculated with Equation 3.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{BIAS} \times IQ(BIAS) + V_{IN} \times IQ(V_{IN}) \quad \text{(EQ. 3)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$, and the maximum expected ambient temperature, $T_{A(MAX)}$, determine the maximum allowable power dissipation, as shown in Equation 4, where $\theta_{JA}$ is the junction-to-ambient thermal resistance.

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 4)}$$

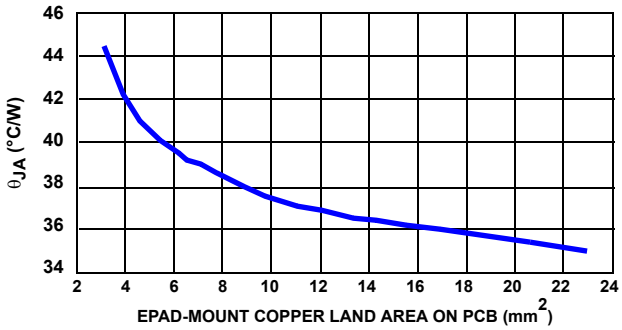



FIGURE 37. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS $\theta_{JA}$ vs EPAD-MOUNT COPPER LAND AREA ON PCB

For safe operation, ensure that power dissipation calculated in Equation 3 ($P_D$) is less than the maximum allowable power dissipation, $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heat sink. For heat sinking, the EPAD of this package must be soldered to the copper plane (GND plane). Figure 37 shows a curve for the $\theta_{JA}$ of the DFN package for different copper area sizes.

## General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

Filling the thermal pad area with vias is recommended. A typical via array is to fill the thermal pad footprint with vias spaced such that they are center on center 3x the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow.

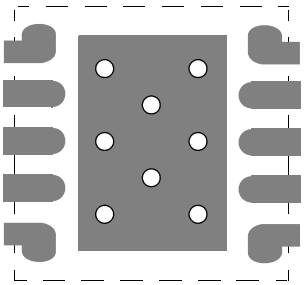


FIGURE 38. PCB VIA PATTERN

Connect all vias to the round plane. For efficient heat transfer, it is important that the vias have low thermal resistance. Do not use “thermal relief” patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane.

# ISL80111, ISL80112, ISL80113 Split Supply LDO Evaluation Board User Guide

## Description

The ISL8011XEVAL1Z provides a simple platform to evaluate performance of the ISL8011X family of split supply LDOs. Jumpers are provided to easily set popular output voltages.

The ISL80111, ISL80112, and ISL80113 are single-output LDOs specified for 1A, 2A, 3A of output current and are optimized for less than 2.5V and less output voltage conversions. The ISL8011X supports $V_{IN}$ voltages down to 1V, provided a standard legacy 3.3V or 5V is applied on the $V_{BIAS}$ pin. The output voltage is adjustable from 0.8V to 3.3V.

An enable input, having a threshold < 1V, allows the part to be placed into a low quiescent current shutdown mode. A submicron CMOS process is utilized for this product family to deliver best-in-class analog performance and overall value for applications in need of input voltage conversions to typically below 2.5V. It also has the superior load transient regulation unique to a NMOS power stage.

These LDOs consume significantly lower quiescent current as a function of load compared to bipolar LDOs. This lower consumption translates into higher efficiency and the ability to consider packages with smaller footprints. The quiescent current has been modestly compromised in design to enable leading class fast load transient response and load regulation.

## What's Inside

- The evaluation kit contains the following:
- The ISL80113EVAL1Z with the appropriate parts installed
- The ISL80111, ISL80112, ISL80113 data sheet

## Test Steps

1. Select the desired output voltage by shorting one of the jumpers from JP2 through JP5.
2. Connect both the BIAS and VIN supplies and the load. Enable the IC using jumper JP6 (bottom position) or via a signal on the center post, observe the output.
3. The shipped configuration is enabled and $V_{OUT}$ = 3.3V.
4. Scope shots taken from ISL8011XEVAL1Z boards.

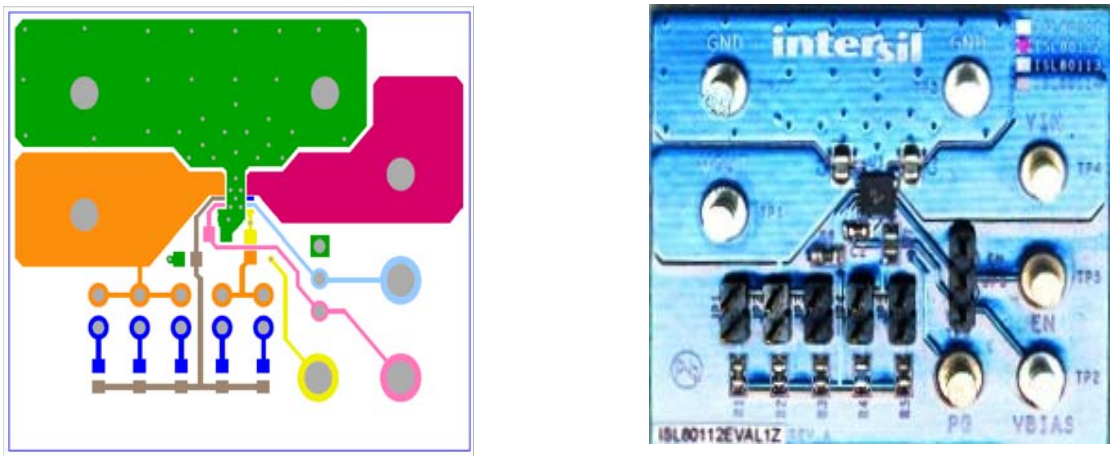
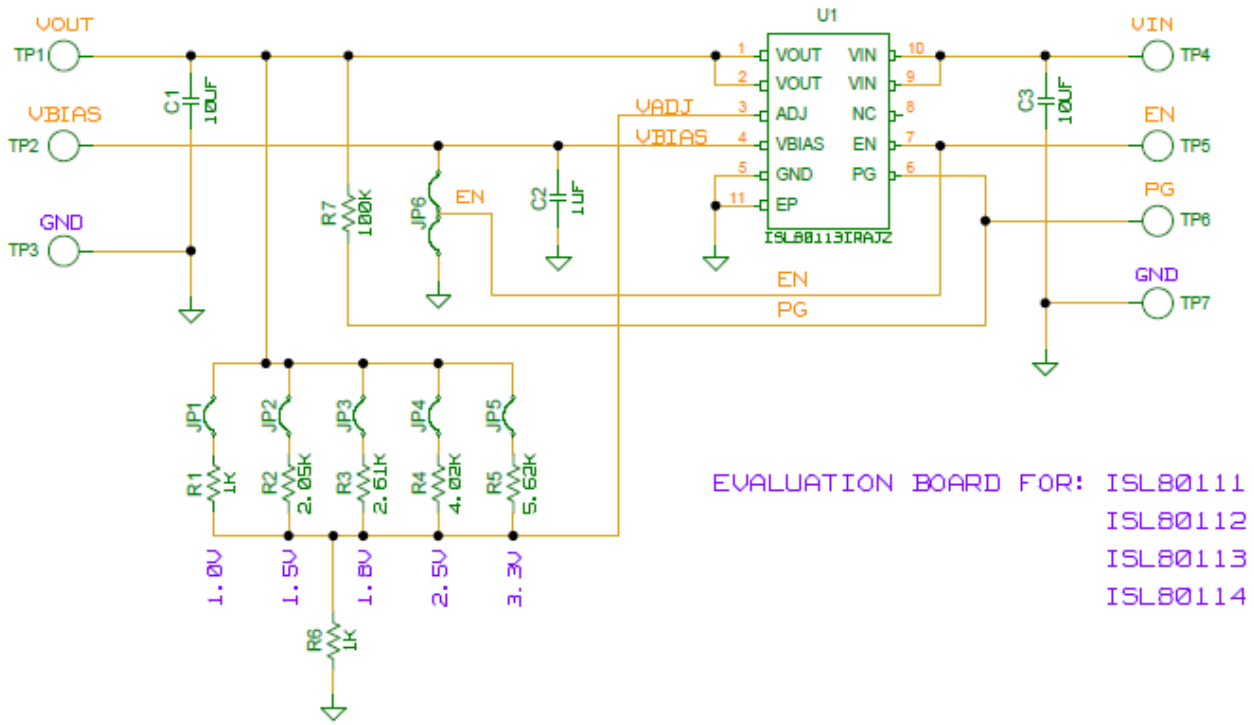



FIGURE 39. ISL80113EVAL1Z (TOP PCB LEFT, PHOTOGRAPH RIGHT)

## Schematic




## Bill of Materials

| REFERENCE DESIGNATOR | VALUE | DESCRIPTION | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| U1 | | ISL80111, ISL80112 or ISL80113 as noted on the evaluation board | Intersil | ISL80111IRAJZ, ISL80112IRAJZ, ISL80113IRAJZ |
| C1, C3 | 10µF | CAP, SMD, 0805, 50V, 10% | Generic | |
| C2 | 1µF | CAP, SMD, 0603 | Generic | |
| R1 | 1kΩ | RES, SMD, 0603, 1% | Generic | |
| R2 | 2.05kΩ | RES, SMD, 0603, 1% | Generic | |
| R3 | 2.61kΩ | RES, SMD, 0603, 1% | Generic | |
| R4 | 4.02kΩ | RES, SMD, 0603, 1% | Generic | |
| R5 | 5.62kΩ | RES, SMD, 0603, 1% | Generic | |
| R6 | 1kΩ | RES, SMD, 0603, 1% | Generic | |
| R7 | 100kΩ | RES, SMD, 0603, 1% | Generic | |
| JP1, JP2, JP3, JP4, JP5, JP6 | | Jumper | Generic | |
| TP1, TP2, TP3 TP4, TP5, TP6 | | Terminal Connector | Generic | |

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| November 1, 2013 | FN7841.2 | Electrical Spec table: Bold the Min and Max values.<br>Page 4- Electrical Spec table title area: Removed “Unless otherwise noted, all parameters are guaranteed over the conditions specified as follows” and replaced by “Unless otherwise specified”.<br>Updated POD to latest revision from rev 7 to rev 8. The changes as follow: Corrected L-shaped leads in Bottom view and land pattern so that they align with the rest of the leads (L shaped leads were shorter) |
| June 5, 2012 | FN7841.1 | Ordering Information table on Page 3: Changed evaluation board names from: ISL80111IRAJEVALZ, ISL80112IRAJEVALZ and ISL80113IRAJEVALZ to ISL80111EVAL1Z, ISL80112EVAL1Z and ISL80113VAL1Z.<br>Changed POD L10.3x3 on Page 17 to latest revision from Rev 6 to Rev 7. Change to POD is as follows: Removed package outline and included center to center distance between lands on recommended land pattern.<br>Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly.<br>Figure 6 VADJ Distribution , corrected "Y" scale units from (0.18, 0.16, 0.14, 0.12, 0.10, 0.08, 0.06, 0.04, 0.02, and 0.00) to (18, 16,14,12,10, 8, 6, 4, 2, and 0).<br>Electrical Specifications table on Page 4 "Added UVLO rising spec to show max of 2.9V so implementation at 3.3V is not a math problem". |
| March 30 2012 | FN7841.0 | Initial Release and Added “UVLO _BIAS _r” spec on pg 4. Modified Figures 13 - 17. |

# About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

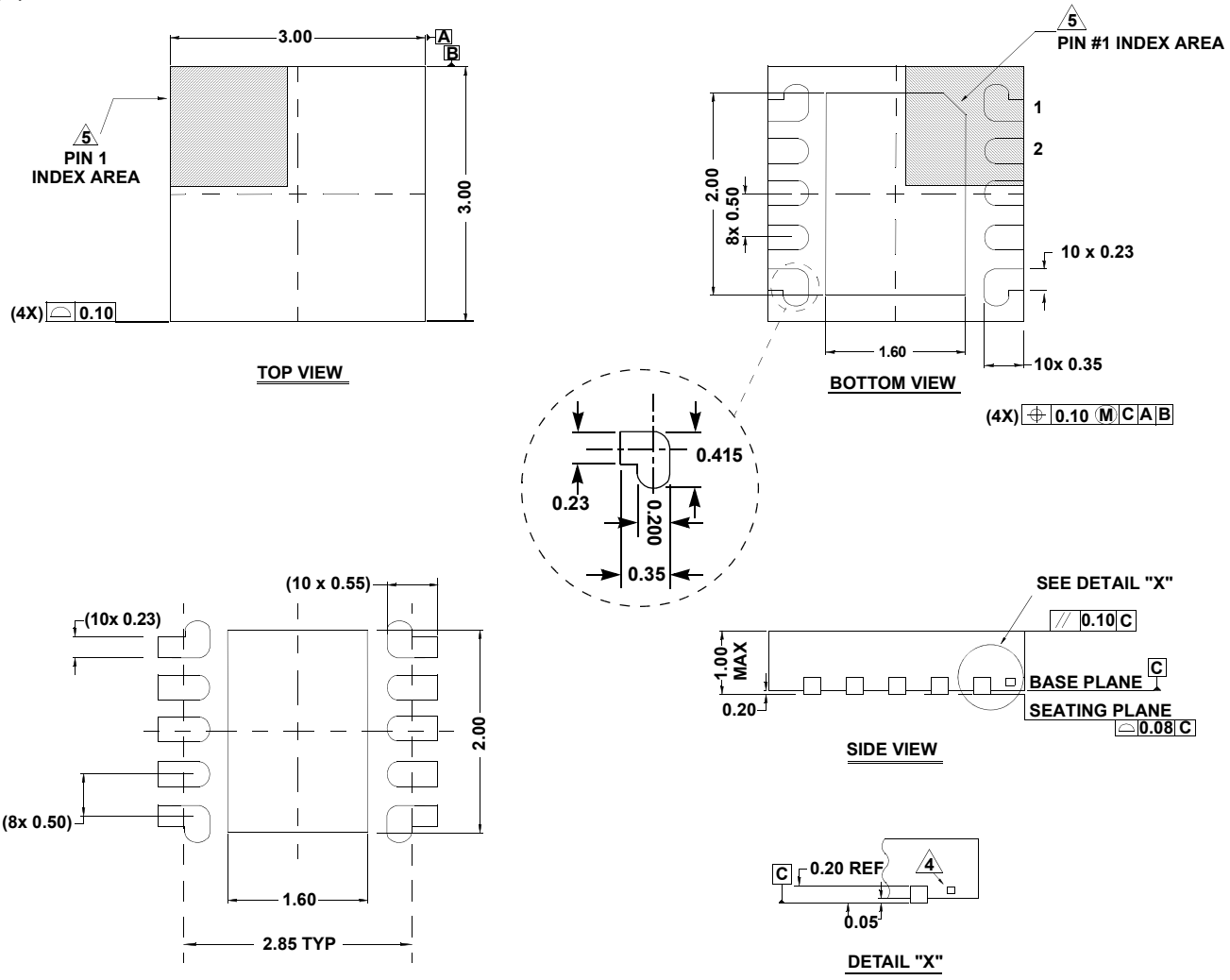
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

# Package Outline Drawing

## L10.3x3

**10 LEAD DUAL FLAT PACKAGE (DFN)**

**Rev 8, 7/12**




**NOTES:**

1. **Dimensions are in millimeters.**
   **Dimensions in ( ) for Reference Only.**
2. **Dimensioning and tolerancing conform to AMSE Y14.5m-1994.**
3. **Unless otherwise specified, tolerance : Decimal ± 0.05**
4. **Tiebar shown (if present) is a non-functional feature.**
5. **The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.**