International
IOR Rectifier

Data Sheet No. PD60062 revO

(NOTE:For new designs, we recommend IR's new product IRS2153D)

IR2153(D)(S)&(PbF)

SELF-OSCILLATING HALF-BRIDGE DRIVER

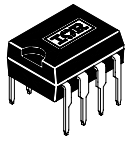
Features

- Integrated 600V half-bridge gate driver
- 15.6V zener clamp on Vcc
- True micropower start up
- Tighter initial deadtime control
- Low temperature coefficient deadtime
- Shutdown feature (1/6th Vcc) on C_T pin
- Increased undervoltage lockout Hysteresis (1V)
- Lower power level-shifting circuit
- Constant LO, HO pulse widths at startup
- Lower di/dt gate driver for better noise immunity
- Low side output in phase with R_T
- Internal 50nsec (typ.) bootstrap diode (IR2153D)
- Excellent latch immunity on all inputs and outputs
- ESD protection on all leads
- Also available LEAD-FREE

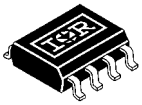
Product Summary

V_{OFFSET}	600V max.
Duty Cycle	50%
T_r/T_p	80/40ns
V_{clamp}	15.6V
Deadtime (typ.)	1.2 µs

Packages



8 Lead PDIP

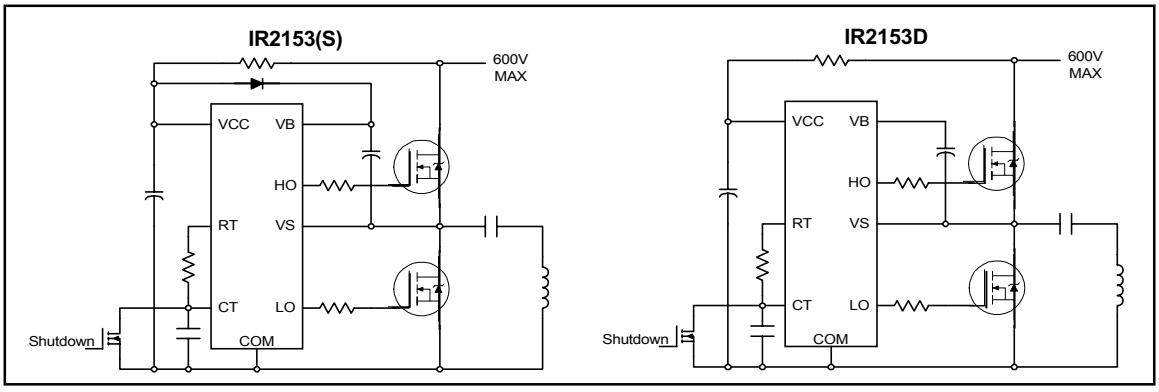


8 Lead SOIC

Description

The IR2153D(S) are an improved version of the popular IR2155 and IR2151 gate driver ICs, and incorporates a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. The IR2153 provides more functionality and is easier to use than previous ICs. A shutdown feature has been designed into the C_T pin, so that both gate driver outputs can be disabled using a low voltage control signal. In addition, the gate driver output pulse widths are the same once the rising undervoltage lockout threshold on V_{CC} has been reached, resulting in a more stable profile of frequency vs time at startup. Noise immunity has been improved significantly, both by lowering the peak di/dt of the gate drivers, and by increasing the undervoltage lockout hysteresis to 1V. Finally, special attention has been payed to maximizing the latch immunity of the device, and providing comprehensive ESD protection on all pins.

Typical Connections



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{RT}	R_T pin voltage		-0.3	V_{CC} + 0.3	
V_{CT}	C_T pin voltage		-0.3	V_{CC} + 0.3	
I_{CC}	Supply current (note 1)		—	25	mA
I_{RT}	R_T pin current		-5	5	
dV_S/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Maximum power dissipation @ $T_A \leq +25°C$	(8 Lead DIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-3.0 (note 2)	600	
V_{CC}	Supply voltage	10	V_{CLAMP}	
I_{CC}	Supply current	(note 3)	5	mA
T_J	Junction temperature	-40	125	°C

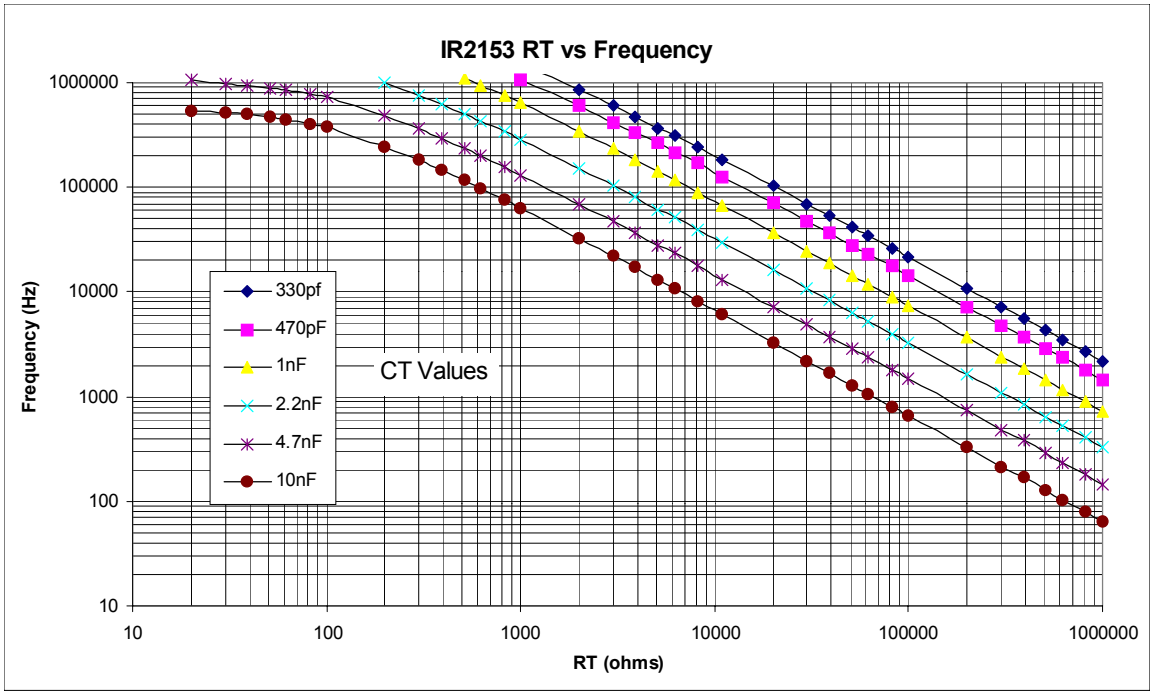
Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Note 2: Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5V.

Note 3: Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6V zener diode clamping the voltage at this pin.

Recommended Component Values

Symbol	Component	Min.	Max.	Units
R_T	Timing resistor value	10	—	kΩ
C_T	C_T pin capacitor value	330	—	pF



Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 12V, C_L = 1000 pF, C_T = 1 nF and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Low Voltage Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	8.1	9.0	9.9	V	
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	7.2	8.0	8.8		
V_{CCUVH}	V_{CC} undervoltage lockout Hysteresis	0.5	1.0	1.5		
I_{QCCUV}	Micropower startup V_{CC} supply current	—	75	150	µA	$V_{CC} \leq V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	—	500	950		
V_{CLAMP}	V_{CC} zener clamp voltage	14.4	15.6	16.8	V	I_{CC} = 5mA

Floating Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{QBSUV}	Micropower startup V_{BS} supply current	—	0	10	µA	$V_{CC} \leq V_{CCUV-}$
I_{QBS}	Quiescent VBS supply current	—	30	50		
V_{BSMIN}	Minimum required V_{BS} voltage for proper functionality from R_T to HO	—	4.0	5.0	V	$V_{CC}=V_{CCUV+}$ + 0.1V
I_{LK}	Offset supply leakage current	—	—	50	µA	$V_B = V_S$ = 600V
VF	Bootstrap diode forward voltage (IR2153D)	0.5	—	1.0	V	IF = 250mA

Oscillator I/O Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
f_{osc}	Oscillator frequency	19.4	20	20.6	kHz	R_T = 36.9kΩ
		94	100	106		R_T = 7.43kΩ
d	R_T pin duty cycle	48	50	52	%	fo < 100kHz
I_{CT}	C_T pin current	—	0.001	1.0	uA	
I_{CTUV}	UV-mode C_T pin pulldown current	0.30	0.70	1.2	mA	V_{CC} = 7V
V_{CT+}	Upper C_T ramp voltage threshold	—	8.0	—	V	
V_{CT-}	Lower C_T ramp voltage threshold	—	4.0	—		
V_{CTSD}	C_T voltage shutdown threshold	1.8	2.1	2.4		
V_{RT+}	High-level R_T output voltage, V_{CC} - V_{RT}	—	10	50	mV	I_{RT} = 100µA
		—	100	300		I_{RT} = 1mA
V_{RT-}	Low-level R_T output voltage	—	10	50		I_{RT} = 100µA
		—	100	300		I_{RT} = 1mA
V_{RTUV}	UV-mode R_T output voltage	—	0	100		$V_{CC} \leq V_{CCUV-}$
V_{RTSD}	SD-Mode R_T output voltage, V_{CC} - V_{RT}	—	10	50		I_{RT} = 100µA, V_{CT} = 0V
		—	10	300		I_{RT} = 1mA, V_{CT} = 0V

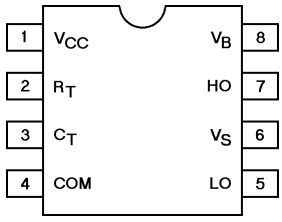
Electrical Characteristics (cont.)

Gate Driver Output Characteristics						
Symbol	**Definition**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
V_{OH}	High level output voltage, V_{BIAS} -V_O	—	0	100	mV	I_O = OA
VOL	Low-level output voltage, VO	—	0	100		I_O = OA
VOL_UV	UV-mode output voltage, VO	—	0	100		I_O = OA $V_{CC} \leq V_{CCUV-}$
t_r	Output rise time	—	80	150	nsec	
t_f	Output fall time	—	45	100		
t_{sd}	Shutdown propogation delay	—	660	—		
t_d	Output deadtime (HO or LO)	0.75	1.20	1.65	µsec	

Lead Definitions

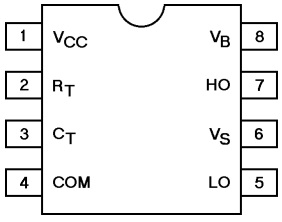
Symbol	Description
V_{CC}	Logic and internal gate drive supply voltage
R_T	Oscillator timing resistor input
C_T	Oscillator timing capacitor input
COM	IC power and signal ground
LO	Low side gate driver output
V_S	High voltage floating supply return
HO	High side gate driver output
V_B	High side gate driver floating supply

Lead Assignments



8 Lead PDIP

IR2153D

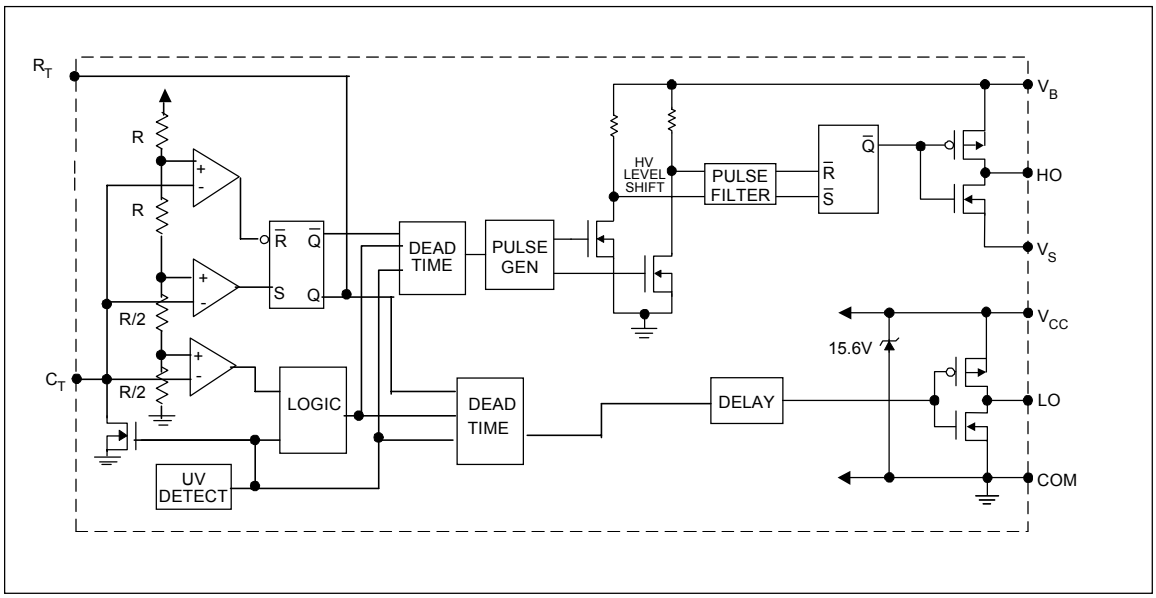


8 Lead SOIC

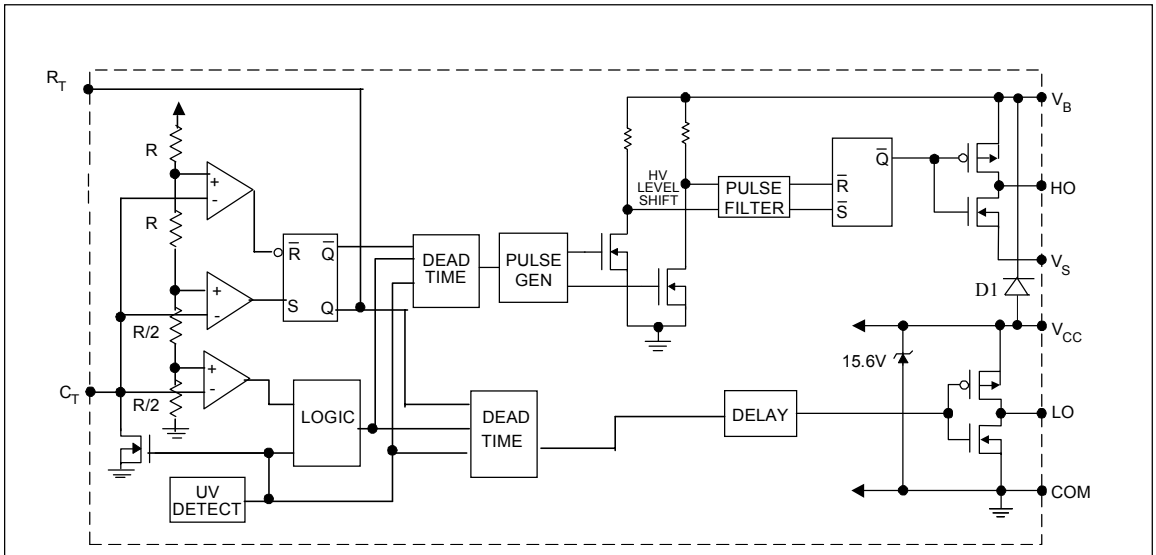
IR2153(S)

NOTE: The IR2153D is offered in 8 lead PDIP only.

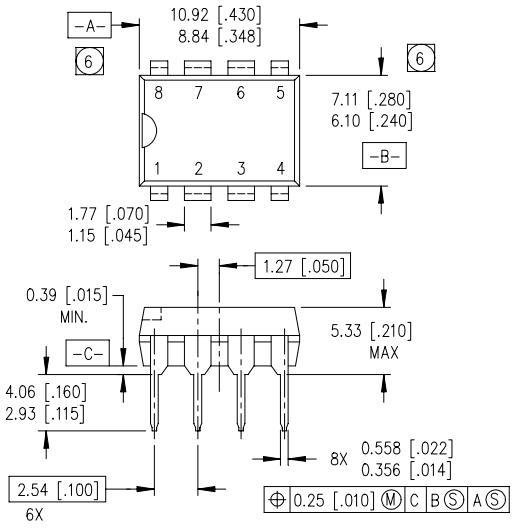
Functional Block Diagram for IR2153(S)



Functional Block Diagram for IR2153D

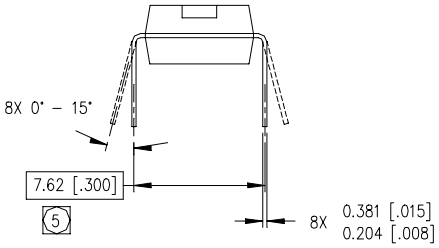


NOTE: The D1 is a separate die.



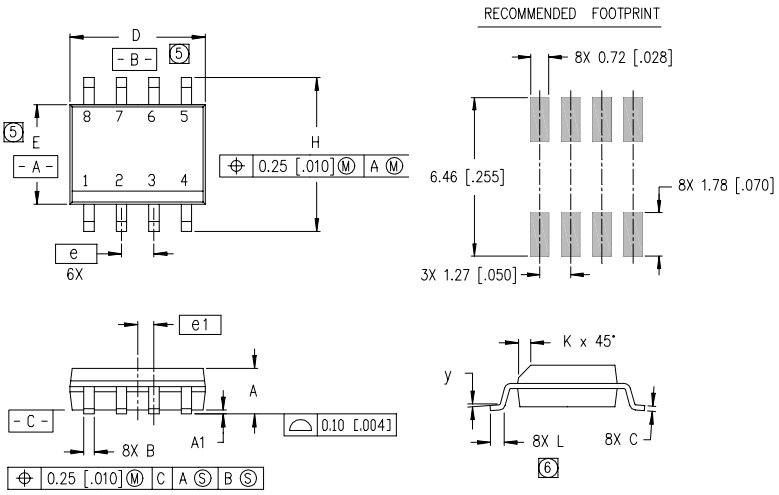
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-0021 08

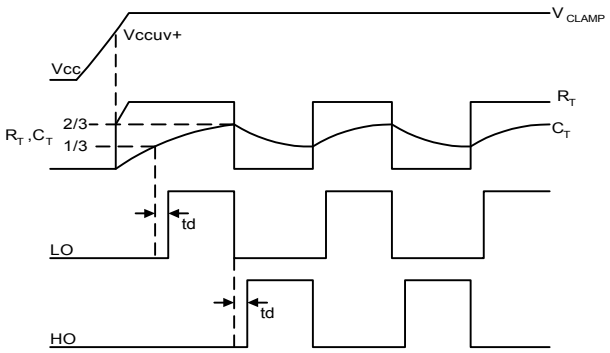


Figure 1. Input/Output Timing Diagram

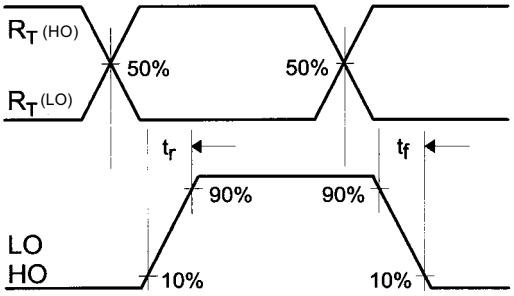


Figure 2. Switching Time Waveform Definitions

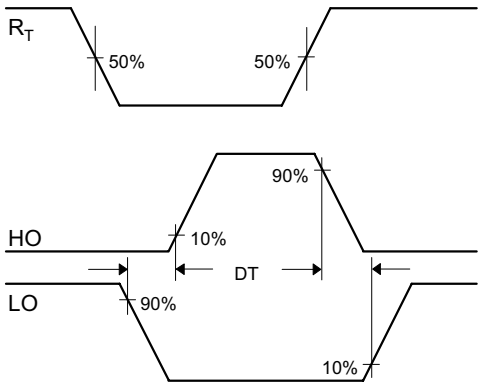
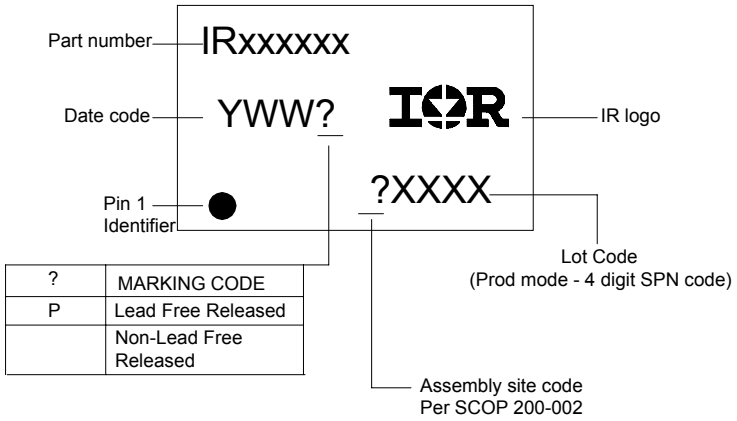


Figure 3. Deadtime Waveform Definitions

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead PDIP IR2153 order IR2153
8-Lead SOIC IR2153S order IR2153S
8-Lead PDIP IR2153D order IR2153D

Leadfree Part
8-Lead PDIP IR2153 order IR2153PbF
8-Lead SOIC IR2153S order IR2153SPbF
8-Lead PDIP IR2153D order IR2153DPbF