() IDT.

PCIE GEN 2/3 & QPI CLOCK FOR ROMLEY-BASED SERVERS

932SQ420D

General Description

The 932SQ420D is a main clock synthesizer for Romley-generation Intel based server platforms. The 932SQ420D is driven with a 25 MHz crystal for maximum performance. It generates CPU outputs of 100 or 133.33 MHz.

Recommended Application

CK420BQ

Output Features

- 4 HCSL CPU outputs
- 4 HCSL Non-Spread SAS/SRC outputs
- 3 HCSL SRC outputs
- 1 HCSL DOT96 output
- 1 3.3V 48M output
- 5 3.3V PCI outputs
- 1-3.3V REF output

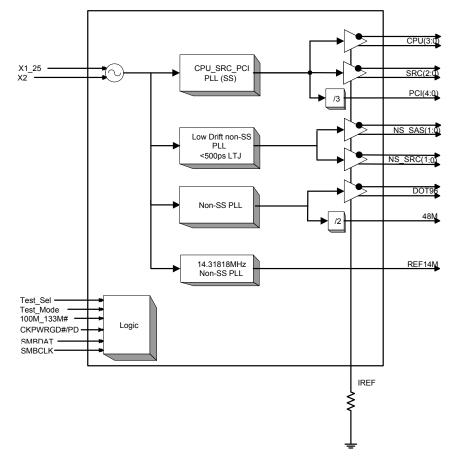
Block Diagram

Features/Benefits

- 0.5% down spread capable on CPU/SRC/PCI outputs/Lower EMI
- 64-pin TSSOP and MLF packages/Space Savings

Key Specifications

- Cycle to cycle jitter: CPU/SRC/NS_SRC/NS_SAS < 50ps.
- Phase jitter: PCIe Gen2 < 3ps rms, Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms
- Phase jitter: NS-SAS < 0.4ps rms using raw phase data
- Phase jitter: NS-SAS < 1.3ps rms using Clk Jit Tool 1.6.3



1

Pin Configuration - 64TSSOP

SMBCLK GND14 AVD14 VDD14 ^v REF14_3x/TEST_SEL GND14 GNDXTAL X1_25 X2_25 VDDXTAL GNDPCI VDDPCI PCI4_2x PCI3_2x PCI2_2x PCI2_2x PCI2_2x PCI2_2x PCI2_2x GNDPCI VDDPCI VDDPCI VDDPCI PCI4_23 PCI2_24 PCI3_24 PCI3_24 PCI3_24 PCI3_25 CXPURDE CXPU	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 24 25 26 27 28 29 30 31	932SQ420	63 62 61 60 59 58 57 56 55 4 3 52 51 50 99 88 77 66 55 54 53 52 51 50 99 88 77 66 55 54 33 73 66 55 54 53 52 51 50 99 88 77 66 55 54 53 52 51 50 99 88 77 66 55 55 55 55 55 55 55 55 55 55 55 55	SMBDAT VDDCPU CPU3T CPU3C CPU2T CPU2C GNDCPU VDDCPU CPU1T CPU1C CPU0T CPU0T CPU0T CPU0C GNDNS AVDD_NS_SAS NS_SAS1T NS_SAS1T NS_SAS1C NS_SAS0T NS_SAS0T NS_SAS0T NS_SAS0T NS_SAS0T NS_SAS0T NS_SAS0T NS_SAS0C GNDNS VDDNS NS_SRC1T NS_SRC0C IREF GNDSRC AVDD_SRC VDDSRC SRC2T SRC2C SRC1T SRC1C
	-	64-TSSOP		1

Note: Pins with ^ prefix have internal 120K pullup Pins with v prefix have internal 120K pulldown

Spread Spectrum Control

SS_Enable	CPU, SRC &
(B1b0)	PCI
0	OFF
1	ON

932SQ420 Power Down Functionality

1 HI-Z ¹ Low Low ²	CKPWRGD#/PD	Differential Outputs	Single-ended Outputs	Single ended Outputs w/Latch		
0 Running	1	HI-Z ¹	Low	Low ²		
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	0	Running				

 Hi-Z on the differential outputs will result in both True and Complement being low due to the termination network
 These outputs are Hi-Z after VDD is applied and before the first assertion of CKPWRGD#.

Power Group Pin Numbers

ML	F	TSSOP		Description	
VDD	GND	VDD	GND	Description	
57	56	3	2	14MHz PLL Analog	
58	60	4	6	REF14M Output and Logic	
64	61	10	7	25MHz XTAL	
2,9	1,8	12, 19	11, 18	PCI Outputs and Logic	
10	12	20	22	48MHz Output and Logic	
16	13	26	23	96MHz PLL Analog, Output and Logic	
19,27	22	29, 37	32	SRC Outputs and Logic	
28	29	38	39	SRC PLL Analog	
35	36	45	46	Non-Spreading Differential Outputs & Logic	
41	42	51	52	NS-SAS/SRC PLL Analog	
47,53	48	57,63	58	CPU Outputs and Logic	

2

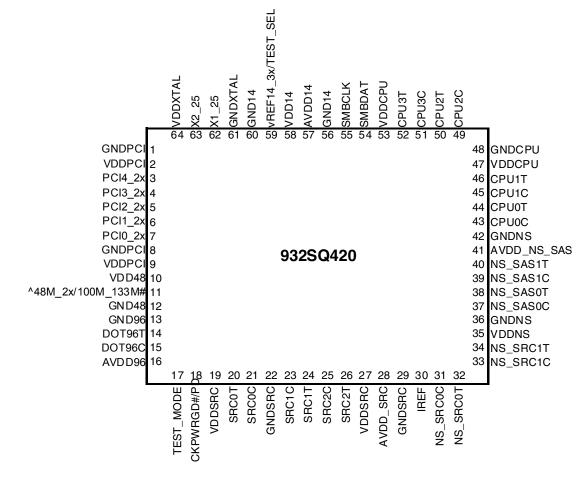
Pin Descriptions - 64 TSSOP

Instrume Description 2 Site CA PMR Description 2 OND14 PMR Description Description 4 VDD14 PMR Description Description 4 VDD14 PMR PMR Description Description 6 OND14 PMR Description Description Description 6 OND14 PMR Description Description Description 6 OND14 PMR Description Description Description 7 ONDXTAL PMR Borung finion Crystal organization Description 7 ONDXTAL PMR Borung finion Description Description 10 NDDXTAL PMR Borung finion Description Description 11 SNDECI PMR Borung finion Description Description 12 VDDPCI PMR Borung finion Description Description Description <		PIN NAME TYPE DESCRIPTION					
2 GND14 PVM Found pin for 14MH2 output and logic. 3 AVXD014 PVM Avxper pin for 14MH2 output and logic. 5 VREF14_3x/TEST_SLL VD 14.318 MH2 reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. 6 GND14 PVM Ground pin for 14MH2 output and logic. 7 GNDXTAL PVM Ground pin for 14MH2 output and logic. 8 X1_25 IN Crystal output, Norminally 25.00MHz. 9 X2_25 OUT Crystal output, Norminally 25.00MHz. 10 VDDXTAL PVM Ground pin for PC outputs and logic. 11 GNDPCI PVM Ground pin for PC outputs and logic. 12 VDDXTAL PVM S3.Y poer for the PC old outputs and logic. 13 GNDPCI PVM S3.Y poer for the PC old outputs and logic. 14 PCI2.2x OUT S3.Y PCI dock output 15 PCI2.2x OUT S3.Y PCI dock output 16 PCI1.2x OUT S3.Y owner for the PCI outputs and logic. 17 PCI0.2x OUT S3.Y AdMHz outputs and logic. 18 <th>PIN #</th> <th></th> <th>TYPE</th> <th colspan="3"></th>	PIN #		TYPE				
3 AVDD14 PWH Rever prior 14MHz PLL 4 VDD14 PWH Rever prior 14MHz and logic PVE 5 vREF14_3x/TEST_SEL IO 14.318 MHz reference clock. 3X drive strength as default / TEST_SEL listched input to enable test mode. Refer to TSE Clarification Table. This pin has a weak (-12080hm) internal pull down. 6 GNDTAL PWH Giound pin for 75410 Sociator. PVE 7 GNDSTAL PWH Giound pin for 75410 Sociator. PVE 8 X1_25 IN Crystal input. Nominaly 25.00MHz. PVE 10 VDDCPCI PWH Giound pin for PCI outputs and logic. PVE PVE 11 GNDPCI PWH Giound pin for PCI outputs and logic. PVE PVE PVE 12 VDDPCI PWH Giound pin for PCI outputs and logic. PVE P							
4 VDD14 PWR Power pin for 14MHz output and logic 5 VREF14_SVTEST_SEL IV0 Refer to Test Clarification Table. This pin has a weak (-120Kohm) internal pull down. 6 KND14 PWR Gound pin for 14MHz output and logic. 7 GNDXTAL PWR Gound pin for 14MHz output and logic. 8 X1.25 IN1 Crystal output, Normially 25:00MHz. 9 X2.25 OUT Crystal output, Normially 25:00MHz. 10 VDDDPC1 PWR 33:V power for the PC1 outputs and logic 11 GNDPC1 PWR 33:V power for the PC1 outputs and logic 12 VDDPC1 PWR 33:V power for the PC1 outputs and logic 13 PC14; 2x OUT 33:V PC1 dock output 14 PC13; 2x OUT 33:V PC1 dock output Test and VDPC1 17 PC14; 2x OUT 33:V PC1 dock output Test and VDPC1 18 ONDPC1 PWR 3:V power for the PC1 outputs and logic. Test and VDPC1 14 PC13; 2x OUT 33:V PC1 dock output and logic. Test and VDPC1 14 PC14; 2x OUT 33:V PC1							
s VREF14_3vTEST_SEL IO 14318 MH z reference clock. 3X drive strength as default / TEST_SEL Lander input to enable test mode. Refer to T28 Clarification Table. This pin has a week (-120Kohm) internal pull down. 6 GND14 PVM B Gound pin for 14MH z output and logic. 1 7 GND3TAL PVM B Gound pin for 14MH z output and logic. 1 8 X1_25 IN Crystal input, Nominally 25 00MHz. 2 10 VDDXTAL PVM B Gound pin for 761 outputs and logic. 1 1 11 GNDFCI PVM B Gound pin for PCI outputs and logic. 1 1 1 12 VDDPCI PVM B Gound pin for PCI outputs and logic. 1	-						
Mich M., 39/165/1942 Work Rev and prior 14MHz output and logic. GND TAL PVME Ground pin for 14MHz output and logic. K1, 25 IN Crystal input, Normially 25.00MHz. VEX.25 OUT Crystal output, Normially 25.00MHz. VEX.25 OUT S3.97 Cl dock output VEX.26 OUT S3.97 Cl dock output	4	VDD14	PWR				
Bit Provide Provide Test Control Table. The print has a week (-120kcom) internal pull down. CRNDTAL PWR Ground prin for 14M/2 output and togic. CRNDTAL PWR Ground prin for 14M/2 output and togic. V1.25 IN Crystal aduptu, Nominally 25 00M/12. V0.261 PWR SX prove for the crystal accilitator. V0.2701 PWR SX prove for the crystal accilitator. V0.2702 PWR SX prove for the crystal accilitator. V0.2701 PWR SX prove for the crystal accilitator. V0.2702 PWR SX prove for the crystal accilitator. V0.2703 PVR SX prove for the crystal accilitator. V0.2704 PWR SX prove for the crystal accilitator. V0.2705 PWR SX prove for the crystal accilitator. V0.2804 OUT SX Prove for the crystal accilitator. V0.2804 OUT SX Prove for the crystal accilitator. V0.2804 PWR SX Prove for the crystal accilitator. V1.2804 PWR SX Prove for the crystal accilitator. V1.2804 PWR SX Prove for the crystal accilita	5	VBEE14 3X/TEST SEL	1/0				
7 GRDXTAL PWR Ground pin for Crystal Deplator. 8 X1_25 IN Crystal Input. Norminally 25:00MHz. 9 X2_25 OUT Crystal output. Norminally 25:00MHz. 10 VDDXTAL PWR I3:37 power for the crystal oscillator. 11 GNDPCI PWR I3:37 power for the crystal oscillator. 12 VDDPCI PWR I3:37 power for the Crystal outputs and logic. 13 PCI4.2x OUT I3:37 PCI clock output 14 PCI3.2x OUT I3:37 PCI clock output 15 PCI2.2x OUT I3:37 PCI clock output 16 PCI2.2x OUT I3:37 PCI clock output 17 PCI0.2x OUT I3:37 PCI clock output 18 GNDPCI PWR I3:37 power for the PCI outputs and logic. 20 VDDPCI PWR I3:37 power for the PCI outputs and logic. 21 ^4BM_2x/100M_133Mi IO there PCI clock output I3:37 KBMHz output and logic. 22 GND48 PWR I3:37 power for the PCI outputs and logic. there PCI clock output I3:37 KBMHz output I1:17 KBMZ output I1:17 KBMZ output I1:17							
8 X1 25 INI Crystal input. Norminally 25 00MHz. 10 VDDXTAL PVR [Gound prior PC) couputs and logic. 11 GNDPCI PVR [Gound prior PC) couputs and logic. 12 VDDPCI PVR [Gound prior PC) couputs and logic. 13 PCIA 2× OUT [33V PC] dock ouput 14 PCIA 2× OUT [33V PC] dock ouput 15 PCIA 2× OUT [33V PC] dock ouput 16 PCIA 2× OUT [33V PC] dock ouput 17 PCIA 2× OUT [33V PC] dock ouput 18 GNDPCI PVR [33V power for the PC] outputs and logic. 19 VDDPCI PVR [33V power for the 48MHz output 30 logic. 19 VDDA8 PVR [33V power for the 48MHz output 30 logic. 20 VDD48 PVR [Gound prior fO? Loutput and logic. 21 ^48M_2x/100M_133M# I/O Intreshotds. This pin has a weak (-120Kom) internal pull up. 1 1 100 threshould and logic. Complementary tocks of differential 96MHz output. These are current mode outputs. These are current mode outputs and logic. 23 GND496 PVR [Gound prior D? DE output and logic. The cock of differential 96MHz output. These are current mode outputs and extemal 3	-						
9 X2_25 OUT Crystal output, Nominally 25.00MHz. 10 VDDXTAL PVM B 33/ power for the Cytal socialitor. 11 GNDPCI PVM B 33/ power for the Cytal outputs and logic. 13 PCI4_2x OUT 33/ PCI dock output 14 PCI3_2x OUT 33/ PCI dock output 15 PCI2_2x OUT 33/ PCI dock output 16 PCI1_2x OUT 33/ PCI dock output 17 PCI0_2x OUT 33/ PCI dock output 18 GNDPCI PVM B Ground pin for PCI outputs and logic. 20 VDD48 PVM B 33/ power for the AMMHz output and logic. 21 ^48M_2x/100M_133M# IO Treshoulds. This pin has a weak (-120KM) internal pull up. 21 ^48M_2x/100M_133M# IO Treshoulds. This pin has a weak (-120KM) internal pull up. 22 GND48 PVM B Ground pin for 4MHz output. These are current mode outputs. These are current mode outputs. 24 DOT961 OUT Treshoulds of differential 9MHz output. These are current mode outputs and exem al 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PVM B 33/ power for the 84/9MHz output. These are current mode o	7	GNDXTAL	PWR	Ground pin for Crystal Oscillator.			
10 VDDXTAL PVM B Ground pin for PC locuputs and logic. 11 GNDPCI PVM B Ground pin for PC locuputs and logic. 12 VDDPCI PVM B Ground pin for PC locuputs and logic. 14 PCI3_2x OUT 3.3V PCI dock output 15 PCI2_2x OUT 3.3V PCI dock output 16 PCI3_2x OUT 3.3V PCI dock output 17 PCI0_2x OUT 3.3V PCI dock output 18 GNDPCI PVM B Ground pin for PCI outputs and logic. 19 VDDPCI PVM B 3.3V power for the 4MMz output and logic. 19 VDDPCI PVM B 3.3V power for the 4MMz output and logic. 10 trestends. This pin has a wask (-120km) internal pull up. 12 VAMA_2X/100M_133M# Iot trestends. This pin has a wask (-120km) internal pull up. 12 GND48 PVM B Ground pin for 2MM1z output and logic. 24 DOT96T OUT Tue clock of differential 9MMz output and logic. 25 DOT96C OUT Tue clock of differential 9MMz output and logic. 26 AVDD86 PVM Ground pin for 2MMMz December PL2 and REFN divider mode while in test mode. Refer to Task fork and the 9MMz output and logic. 27 TEST_MODE	8		IN	Crystal input, Nominally 25.00MHz.			
11 GNDPCI PVMB 33V power for the PCI outputs and logic. 13 PCI4_2X OUT 33V PCI dock output 14 PCI3_2X OUT 33V PCI dock output 15 PCI4_2X OUT 33V PCI dock output 16 PCI1_2X OUT 33V PCI dock output 17 PCI0_2X OUT 33V PCI dock output 18 GNDPCI PVMB 33V power for the PCI outputs and logic. 19 VDDPCI PVMB 33V power for the PCI outputs and logic. 20 VDD44 PVM 33V power for the PCI outputs and logic. 21 ~48M_2x/100M_133M# I/O thresholds. This pin has a weak (~120Kom) internal pull up. 22 GND48 PVMF Ground pin for PCI9 output and logic. thresholds. This pin has a weak (~120Kom) internal pull up. 23 GND96 PVMF Ground pin for AdMHz output and logic. thresholds. The Sec values for the administry output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49 ohm shunt resistors are required for termination. 24 D0T96T OUT and external 32 GMNSe developed for the 369GMHz output. These are current mode outputs and external 33 ohm series resistors and 49 ohm shunt resistors are required for termination. 26 DDT96C OUT fast faref	9	X2_25	OUT	Crystal output, Nominally 25.00MHz.			
12 VDDPCI PVH 3: 3V power for the PCI outputs and logic 13 PCI4 2x OUT 3: VPCI dock output 14 PCI3 2x OUT 3: VPCI dock output 15 PCI2 2x OUT 3: VPCI dock output 16 PCI1 2x OUT 3: VPCI dock output 17 PCIO 2x OUT 3: VPCI dock output 18 GNDPCI PVH 3: SV power for the PCI outputs and logic. 19 VDDPCI PVH 3: SV power for the AMHz output and logic. 20 VDD48 PVH 3: SV power for the PCI outputs and logic. 21 ^48M_2x/100M_133M# I/O thresholds. This pin has a weak (~120Korn) internal pull up. 22 GND48 PVH Ground pin for DO196 output and logic. SV 48MHz output 3: SV dollard and logic. 23 GND48 PVH Ground pin for DO196 output and logic. The colock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 3: 3 ohm series resistors and 49. ohm shunt resistors are required for termination. 24 DOT96C OUT The SCH ook of differential 96MHz output. These are current mode outputs and external 3: ohm series resistors and 49. ohm shunt resistors are required for termination. 25 DOT96C OUT TesCLandration Table.	10	VDDXTAL	PWR	3.3V power for the crystal oscillator.			
13 PCId 2x OUT 33V PCI dock output 14 PCIB 2x OUT 33V PCI dock output 15 PCIE 2x OUT 33V PCI dock output 16 PCII 2x OUT 33V PCI dock output 17 PCIO 2x OUT 33V PCI dock output 18 GNDPCI PWR 32V PCI dock output 19 VDDPCI PWR 33V power for the PCI outputs and logic. 20 VDD48 PWR 33V power for the PCI outputs and logic. 21 ^48M 2x/100M_133M# IO thresholds. This pin has a weak (-120Kom) internal pull up. 1 -1 10MHz, 0 = 133MHz operating frequency 1 22 GND48 PWR Ground p for CDT8 output and logic. 23 GND96 PWR Ground p for CDT8 output and logic. 24 D0T96T OUT advermal 33 Ohm series resistors and 49.0 ohm shunt resistors are required for termination. 25 D0T96C OUT advermal 33 Ohm series resistors and 49.0 ohm shunt resistors are required for termination. 26 AVDD66 PWR 33V power for the 48%6MLz PLL and the 96MHz output and logic 1 27 TEST_MODE IN TEST_MODE	11	GNDPCI	PWR	Ground pin for PCI outputs and logic.			
14 PCI3_2x OUT 33V PCI dock output 15 PCI2_2x OUT 33V PCI dock output 16 PCI1_2x OUT 33V PCI dock output 17 PCI0_2x OUT 33V PCI dock output 18 GNDFCI PWR Borund ph for PCI outputs and logic 19 VDDP4 PWR 33V power for the PCI outputs and logic 20 VDD48 PWR 33V power for the PCI outputs and logic 21 V48M_2x/100M_133Mt I/O 33V 48MHz output and logic 22 GND48 PWR Ground ph for 48MHz output and logic. 23 VDD44 PWR Ground ph for D0T96 output. These are current mode outputs. 24 D0T96T OUT Testick of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 25 D0T96C OUT Test_MODE NT Test_MODE IN 18 Test_MODE IN TEST_MODE IN SV power for the 4896MHz PL and the 96MHz output and logic 27 TEST_MODE IN SV pOWER for the A896MHz PL and the 96MHz output and logic IN 28 VDD	12	VDDPCI	PWR	3.3V power for the PCI outputs and logic			
15 PCI2_2x OUT 33V PCI dock output 16 PCII_2x OUT 33V PCI dock output 17 PCI0_2x OUT 33V PCI dock outputs and logic. 18 GNDPCI PWR 33V PCI dock outputs and logic. 20 VDDFCI PWR 33V power for the PCI outputs and logic. 21 ^48M_2v/100M_133M# I/O assW adM1z output and logic. 22 GND48 PWR Ground pt for AMM1z output and logic. 23 GND48 PWR Ground pt for AMM1z output and logic. 24 D0T96T OUT Tue clock of differential 6MHz output and logic. 25 D0T96C OUT Tue clock of differential 6MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 D0T96C OUT TesT_MODE TEST_MODE TEST_MODE is a real time input to select between H-iZ and REF/N divider mode while in test mode. Refer to test as resistors and 49.9 ohm shunt resistors are required for termination. 27 TEST_MODE IN TeST_MODE is a real time input to select between H-iZ and REF/N divider mode while in test mode. Refer to test calification Table. 28 CKPWRGD#/PD IN	13	PCI4_2x	OUT	3.3V PCI clock output			
15 PCI2_2x OUT 33V PCI dock output 16 PCII_2x OUT 33V PCI dock output 17 PCI0_2x OUT 33V PCI dock outputs and logic. 18 GNDPCI PWR 33V PCI dock outputs and logic. 20 VDDFCI PWR 33V power for the PCI outputs and logic. 21 ^48M_2v/100M_133M# I/O assW adM1z output and logic. 22 GND48 PWR Ground pt for AMM1z output and logic. 23 GND48 PWR Ground pt for AMM1z output and logic. 24 D0T96T OUT Tue clock of differential 6MHz output and logic. 25 D0T96C OUT Tue clock of differential 6MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 D0T96C OUT TesT_MODE TEST_MODE TEST_MODE is a real time input to select between H-iZ and REF/N divider mode while in test mode. Refer to test as resistors and 49.9 ohm shunt resistors are required for termination. 27 TEST_MODE IN TeST_MODE is a real time input to select between H-iZ and REF/N divider mode while in test mode. Refer to test calification Table. 28 CKPWRGD#/PD IN	14	PCI3_2x	OUT	3.3V PCI clock output			
16 PCI1_2x OUT 3.3V PCI dock output 17 PCI0_2x OUT 3.3V PCI dock output 18 GNDPCI PVM Ground pin for PCI outputs and logic. 19 VDDP4 PVM Ground pin for PCI outputs and logic. 20 VDD48 PVM 3.3V power for the 48MHz output and logic. 3.3V 48MHz output 3.3V loterant CPU forequency select latched input pin. See ViFS and VihFS values for 10 thresholds. This pin has a weak (-120Kom) internal pull up. 11 100 thresholds. This pin has a weak (-120Kom) internal pull up. 22 GND48 PVM Ground pin for 44MHz output and logic. 23 GND96 PVM Ground pin for 44MHz output and logic. 24 D0T96T Output Tese are current mode outputs. These are current mode outputs. These are current mode outputs. These are current mode outputs. 24 D0T96C OUT TeST_MODE PVM 3.3V power for the 4896MHz PLL and the 96MHz output and logic. 27 TEST_MODE IN TEST_MODE is a real lime input to select between H-2 and HE-FN divider mode while in test mode. Refer to Test 02 affication Table. 28 VDDSRC PVM 8.3V power for the SRC output. These are current mode outputs and external 33 ohm series resistors and 4.9.0 ohm shunt resistors are required to	15						
17 PCI0_Zx OUT 3.3V PCI deck output 18 GNDPCI PWR Bround pit for PCI outputs and logic. 19 VDDPCI PWR 3.3V power for the PCI outputs and logic. 20 VDD48 PWR 13.3V power for the PCI outputs and logic. 21 ^48ML_Zv100M_133M# I/O the PCI outputs and logic. 22 GND48 PWR Bround pit for PCI outputs and logic. The sholds. This pin has a weak (-120Kom) internal pull up. 1 1 1 1 1 1 23 GND48 PWR Bround pit for PCI 96 output and logic. The clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shurt resistors are required for termination. 25 DOT96C OUT Test_MODE TEST_MODE TEST_MODE is a real time input to select between H-Z and REF/N divider mode while in test mode. Refer to N res stopped. 26 KFWRGD#/PD N asquertorine Ha96MHz PL, and the 96MHZ output and logic. 27 TEST_MODE IN TEST_MODE is an active low input used to sample latched inputs and allow the device to Power Up. PD is an active low input used to sample latched inputs and allow the device to Power Up. PD is an active low high input pin used to put the device into a low power state. The internal clocks and PL are stopped.<	16		OUT	3.3V PCI clock output			
18 GNDPCI PWR Ground pin for PCI outputs and logic. 19 VDDP6I PWR 3.3V power for the 48MHz output and logic 20 VDD48 PWR 3.3V power for the 48MHz output and logic 21 ^448M_2x/100M_133M# I/V 3.3V 48MHz output 3.3V loterant CPU frequency select latched input pin. See VIFS and VihFS values for 22 GND48 PWR Ground pin for 44MHz output 3.4V loterant CPU frequency select latched input pin. See VIFS and VihFS values for 23 GND46 PWR Ground pin for 44MHz output and logic. 24 DOT961 OUT True clock of differential 96MHz output and logic. 25 DOT96C OUT Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PVR 3.3V power for the 4896MHz PLL and the 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 27 TEST_MODE IN TEST_MODE is an adthe low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL are clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and		_					
19. VDDPCI PWR 3.3V power for the PGI outputs and logic 20 VDD48 PWR 3.3V power for the PAML output and logic. 21 v48M_2x/100M_133M IO thresholds. This pin has a weak (-120Kom) internal pull up. 21 v48M_2x/100M_133M IO thresholds. This pin has a weak (-120Kom) internal pull up. 22 GND48 PWR Ground pin for VD196 output and logic. 23 GND96 PWR Ground pin for OD196 output and logic. 24 DOT96T OUT True clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors are required for termination. 25 DOT96C OUT True clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 4996MHz PLL and the 96MHz output and logic. 27 TEST_MODE IN TEST_MODE is a real time input to select between H-Z and REF/N divider mode while in test mode. Refer to Test Clacification Table. 28 VDDSRC PWR 3.3V power for the SRC outputs and logic. 30 SRC0T OUT True clock of differential SRC output. These are current mode outpu							
20 VDD48 PWR 3.3V power for the 48MHz output and logic. 21 \48M_2x/100M_133M# \VO 3.3V 48MHz output 3.3V tolerant CPU frequency select latched input pin. See VIFS and VIhFS values for thresholds. This pin has a weak (-120Kom) internal pull up. 1 = 100MHz, 0 = 133MHz operating frequency 2 22 GND48 PWR Ground pin for 48MHz output 1. These are current mode outputs. These are current mode outputs and external 30 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 23 DOT96T OUT The clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 24 DOT96C OUT Complementary clock of differential 96MHz output not select between Hi-2 and REF/N divider mode while in test mode. Refer to Test Clanfication Table. 26 AVDD96 PWR 3.3V power for the 8RC output to select between Hi-2 and REF/N divider mode while in test mode. Refer to Test Clanfication Table. 27 TEST_MODE IN TEST_MODE to SRC OUT Tue clock of differential SRC output to select between Hi-2 and REF/N divider mode while in test mode. Refer to Test Clanfication Table. 29 VDDSRC PWR 3.3V power for the SRC output and logic. 30 SRC0T OUT True clock of differential SRC output. T							
21 48M_2x/100M_133M# I/O 3.3V 48MHz output 3.3V tolerant CPU frequency select latched input pin. See VIIFS and VIhFS values for 21 48M_2x/100M_133M# I/O thresholds. This pin has a weak (~120Kom) internal pull up. 22 GND48 PVMR Ground pin for 48MHz output and logic. 22 GND96 PVMR Ground pin for 100T96 output and logic. 24 D0196T OUT Thre clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PVMR Ground pin for the 4396MHz PL Land the 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 27 TEST_MODE I/N TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Trest Carification Table. 28 CKPWRGD#/PD I/N CKPWRGD#/ED I/N 30 SRC0T OUT The clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs. And external 33 ohm series r							
21 ^48M_2x/100M_133M# I/O thresholds. This pin has a weak (-120Kom) internal pull up. 1 = 000H1z, 0 = 133M1z operating frequency 22 GND46 PVR Ground pin for 48M1z output and logic. 23 GND96 PVR Ground pin for 0000 bit of 48M1z output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 24 DOT96C OUT Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PVR 3.3V power for the 4896MHz PLL and the 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-z and REF/N divider mode while in test mode. Refer to Test Clanfication Table. 28 CKPWRGD#/PD IN Say power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for terminati	20	100+0	I VVII				
Intervention Intervention 22 GND48 PWR Ground pin for 48MHz output and logic. 23 GND96 PWR Ground pin for 48MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 24 DOT96T OUT True clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 25 DOT96C OUT Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR B.3V power for the 4896MHz PLL and the 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 27 TEST_MODE N TEST_MODE is a real time input to select between H-Z and REF/N divider mode while in test mode. Refer to track Christian Table. 28 CKPWRGD#/PD N asynchronous active high input pin used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLi are stopped. 29 VDDSRC PWR 3.3V power for the SRC output. These are current mode outp	21	AARM 2x/100M 133M#	1/0				
22 GND48 PWR Ground pin for 48MHz output and logic. 23 GND96 PWR Ground pin for DD76 output and logic. 24 DOT96T OUT True clock of differential 98MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 25 DOT96C OUT Complementary clock of differential 98MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 48/96MHz PLL and the 96MHz output and logic 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 28 CKPWRGD#/PD IN TEST_MODE is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL are stopped. 30 SRC0T OUT Tue clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Tue clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required fo	21	⁴ 40101_2X/100101_133101#	1/0				
23 GND96 PWR Ground pin for DOT96 output and logic. 24 DOT96T OUT The clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 25 DOT96C OUT Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 48/96MHz PLL and the 96MHz output and logic. 27 TEST_MODE IN Test Clafification Table. 28 CKPWRGD#/PD IN Test Clafification Table. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic. 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 33 SRC1C OUT Complementary clock of differential SRC outpu	00						
24 DOT96T Out The clock of differential 96MHz output. These are current mode outputs. These are outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 25 DOT96C Out Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 4396MeX PLL and the 96MHz put and logic. 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 28 CKPWRGD#/PD IN Asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL are stopped. 29 VDDSRC PWR 3.5V power for the SRC outputs and logic The clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C Out Tune clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 33 SRC1C Out Complementary clock							
24 DOT961 OUT and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 25 DOT96C OUT Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 48/96MHz PLL and the 96MHz output and logic 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 28 CKPWRGD#/PD IN asynchronous active high input pin used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL are stopped. 29 VDDSRC PVR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm	23	GIND96	PWR	Ground pin for DO 196 output and logic.			
25 DOT96C Out Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 49/96MHz PLL and the 96MHz output and logic 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 28 CKPWRGD#/PD IN CKPWRGD#/PD EXPUNCE 30 SRC0T OUT CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL: are stopped. 30 SRC0T OUT Tue clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors ar	24	DOT96T	OUT				
25 D0196C 001 series resistors and 49.9 ohm shunt resistors are required for termination. 26 AVDD96 PWR 3.3V power for the 48/96MHz PLL and the 96MHz output and logic 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 28 CKPWRGD#/PD IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 29 VDDSRC PVR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PVR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1C OUT True clock of differential SRC output. These are current mode outputs and external 33 o							
26 AVDD96 PWR 3.3V power for the 49/96MHz PLL and the 96MHz output and logic 27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Claffication Table. 28 CKPWRGD#/PD IN asynchronous active high input pin used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLL: are stopped. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm serie	25	DOT96C	OUT				
27 TEST_MODE IN TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. 28 CKPWRGD#/PD IN CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC1T OUT True clock of differentia							
27 Test Clarification Table. 28 CKPWRGD#/PD IN Test Clarification Table. 28 CKPWRGD#/PD IN asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. <tr< td=""><td>26</td><td>AVDD96</td><td>PWR</td><td></td></tr<>	26	AVDD96	PWR				
1 1	27	TEST MODE	IN				
28 CKPWRGD#/PD IN asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs an							
are stopped. 29 VDDSRC PWR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2C OUT <							
29 VDDSRC PWR 3.3V power for the SRC outputs and logic 30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT Complementary clock of differential SRC output. These are current mode outpu	28	CKPWRGD#/PD	IN	asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs			
30 SRC0T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC1T OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDS OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shun							
30 SRC01 OUT external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VD	29	VDDSRC	PWR	3.3V power for the SRC outputs and logic			
30 SRC01 OUT external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 31 SRC0C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VD				True clock of differential SPC output. These are current mode outputs. These are current mode outputs and			
31 SRC0C Out Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC1C OUT True clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for	30	SRC0T	OUT				
31 SRC0C OUT series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC outputs and logic. 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a <td></td> <td></td> <td></td> <td>external 33 onm series resistors and 49.9 onm snunt resistors are required for termination.</td>				external 33 onm series resistors and 49.9 onm snunt resistors are required for termination.			
31 SRC0C OUT series resistors and 49.9 ohm shunt resistors are required for termination. 32 GNDSRC PWR Ground pin for SRC outputs and logic. 33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC outputs and logic. 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a <td>01</td> <td>00000</td> <td></td> <td>Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm</td>	01	00000		Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm			
32GNDSRCPWRGround pin for SRC outputs and logic.33SRC1COUTComplementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.34SRC1TOUTTrue clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.35SRC2COUTComplementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.36SRC2TOUTComplementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and series resistors and 49.9 ohm shunt resistors are required for termination.37VDDSRCPWR3.3V power for the SRC outputs and logic.38AVDD_SRCPWR3.3V power for the SRC outputs and logic.39GNDSRCPWRGround pin for SRC outputs and logic.40IREFOUTThis pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor ied to ground in order to establish the appropriate current. 475 ohms is the standard	31	30000					
33 SRC1C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC outputs and logic. 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a	32	GNDSRC	PWR				
33 SRC1C OUT series resistors and 49.9 ohm shunt resistors are required for termination. 34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC outputs and logic. 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard							
34 SRC1T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	33	SRC1C	001				
34 SRC11 OUT external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard							
35 SRC2C OUT Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT Complementary clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	34	SBC1T	ОПТ				
35 SRC2C OUT series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	04			external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.			
35 SRC2C OUT series resistors and 49.9 ohm shunt resistors are required for termination. 36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard				Complementary clock of differential SBC output. These are current mode outputs and external 33 ohm			
36 SRC2T OUT True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	35	SRC2C	OUT				
36 SRC21 OUT external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination. 37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	series resistors and 49.9 onm shunt resistors are required for termination.						
37 VDDSRC PWR 3.3V power for the SRC outputs and logic 38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	200	CDCOT					
38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	30	011021	external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
38 AVDD_SRC PWR 3.3V power for the SRC PLL analog circuits 39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 IREF OUT fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	27			2 2)/ nowar far the CPC outputs and logic			
39 GNDSRC PWR Ground pin for SRC outputs and logic. 40 This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard							
40 IREF OUT This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard							
40 IREF OUT fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard	39	GNDSHC	PWR	Ground pin for SHC outputs and logic.			
value.	40	IKEF	OUT				
				Ivalue.			

Pin Descriptions - 64 TSSOP(cont.)

	Beccomptione	• • •						
41	NS_SRC0C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
42	NS_SRC0T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
43	NS_SRC1C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
44	NS_SRC1T	Ουτ	True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
45	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic					
46	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.					
47	NS_SAS0C	OUT	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
48	NS_SAS0T	ОUT	True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
49	NS_SAS1C	OUT	Complementary clock of differential non-spreading SAS output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
50	NS_SAS1T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
51	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.					
52	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.					
53	CPU0C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
54	CPU0T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
55	CPU1C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
56	CPU1T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
57	VDDCPU		3.3V power for the CPU outputs and logic					
58	GNDCPU	PWR	Ground pin for CPU outputs and logic.					
59	CPU2C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
60	CPU2T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
61	CPU3C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
62	CPU3T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.					
63	VDDCPU	PWR	3.3V power for the CPU outputs and logic					
	SMBDAT		Data pin of SMBUS circuitry, 5V tolerant					
64	SIVIBUAT							

Pin Configuration - 64 MLF



Note: Pins with ^ prefix have internal 120K pullup Pins with v prefix have internal 120K pulldowm

Pin Descriptions - 64 MLF

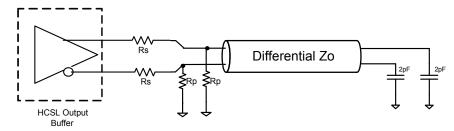
PIN #	PIN NAME	TYPE DESCRIPTION					
	GNDPCI		Ground pin for PCI outputs and logic.				
	VDDPCI		3.3V power for the PCI outputs and logic				
	PCI4_2x		3.3V PCI clock output				
	PCI3 2x						
	PCI2_2x		3V PCI clock output				
	PCI1 2x		3V PCI clock output 3V PCI clock output				
	PCI0_2x		3.3V PCI clock output				
			Ground pin for PCI outputs and logic.				
			3.3V power for the PCI outputs and logic				
10	VDD48	PWR	3.3V power for the 48MHz output and logic				
11	^48M_2x/100M_133M#	3.3V 48MHz output/ 3.3V tolerant CPU frequency select latched input pin. See ViIFS and VihF I/O thresholds. This pin has a weak (~120Kom) internal pull up.					
			1 = 100MHz, 0 = 133MHz operating frequency				
12	GND48	PWR	Ground pin for 48MHz output and logic.				
13	GND96	PWR	Ground pin for DOT96 output and logic.				
14	DOT96T	OUT	True clock of differential 96MHz output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
			Complementary clock of differential 96MHz output. These are current mode outputs and external 33 ohm				
15	DOT96C	OUT	series resistors and 49.9 ohm shunt resistors are required for termination.				
16	AVDD96	PWR					
10	AVDD98	FWN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to				
17	TEST_MODE	IN					
			Test Clarification Table. CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an				
10		INI					
18	CKPWRGD#/PD	IN	asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs				
10	VDD0D0		are stopped.				
19	VDDSRC	PWR	3.3V power for the SRC outputs and logic				
20	SRC0T	OUT	True clock of differential SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
21	SRC0C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
22	GNDSRC	PWR					
			Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series				
23	SRC1C	OUT	resistors and 49.9 ohm shunt resistors are required for termination.				
			True clock of differential SRC output. These are current mode outputs. These are current mode outputs and				
24	SRC1T	OUT	external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
			Complementary clock of differential SRC output. These are current mode outputs and external 33 ohm series				
25	SRC2C	OUT	resistors and 49.9 ohm shunt resistors are required for termination.				
			True clock of differential SRC output. These are current mode outputs. These are current mode outputs and				
26	SRC2T	OUT	external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
07	VDDSRC	DW/D					
	AVDD SRC		3.3V power for the SRC outputs and logic				
			3.3V power for the SRC PLL analog circuits				
29	GNDSRC	PWR					
30	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.				
31	NS_SRC0C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
32	NS_SRC0T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
33	NS_SRC1C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				
34	NS_SRC1T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs. These are current mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.				

Pin Descriptions - 64 MLF (cont).

35	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
36	GNDNS		Ground pin for non-spreading differential outputs and logic.
07		Ουτ	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external
37	NS_SAS0C	001	33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
			True clock of differential non-spreading SAS output. These are current mode outputs. These are current
38	NS_SAS0T	OUT	mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
			Complementary clock of differential non-spreading SAS output. These are current mode outputs and external
39	NS_SAS1C	OUT	33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
			· ·
40	NS_SAS1T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs. These are current
10		001	mode outputs and external 33 ohm series resistors and 49.9 ohm shunt resistors are required for termination.
41	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
42	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
43	CPU0C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series
43	CPUUC	001	resistors and 49.9 ohm shunt resistors are required for termination.
44	CPUOT	Ουτ	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors
44	CF001	001	and 49.9 ohm shunt resistors are required for termination.
45	CPU1C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series
40		001	resistors and 49.9 ohm shunt resistors are required for termination.
46	CPU1T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors
			and 49.9 ohm shunt resistors are required for termination.
47	VDDCPU		
48	GNDCPU	PWR	Ground pin for CPU outputs and logic.
49	CPU2C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series
			resistors and 49.9 ohm shunt resistors are required for termination.
50	CPU2T	OUT	True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors
			and 49.9 ohm shunt resistors are required for termination.
51	CPU3C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external 33 ohm series
			resistors and 49.9 ohm shunt resistors are required for termination. True clock of differential CPU output. These are current mode outputs and external 33 ohm series resistors
52	CPU3T	OUT	and 49.9 ohm shunt resistors are required for termination.
53	VDDCPU		3.3V power for the CPU outputs and logic
53	SMBDAT		Data pin of SMBUS circuitry, 5V tolerant
55	SMBCLK	IN IN	Clock pin of SMBUS circuitry, 5V tolerant
56	GND14		Ground pin for 14MHz output and logic.
57	AVDD14		Analog powerpin for 14MHz PLL
58	VDD14		Power pin for 14MHz output and logic
			14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer
59	vREF14_3x/TEST_SEL	I/O	to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
60	GND14	PWR	Ground pin for 14MHz output and logic.
61	GNDXTAL		Ground pin for Crystal Oscillator.
62	X1_25	IN	Crystal input, Nominally 25.00MHz.
63	X2_25	OUT	Crystal output, Nominally 25.00MHz.
64	VDDXTAL	PWR	3.3V power for the crystal oscillator.

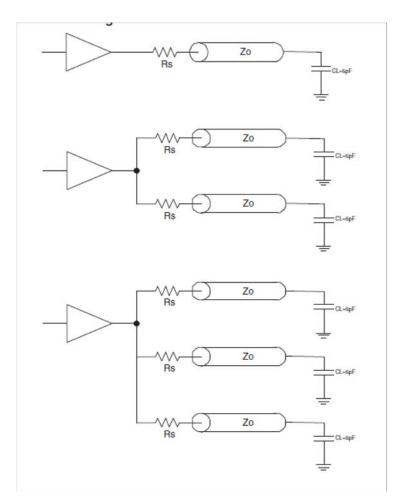
Test Loads and Recommended Terminations

932SQ420 Differential Test Loads



Differe	ntial	Out	tput Te	rmination	Table	
	<i>(</i> 0)			- (0)	_	

DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.3 or 43.2



Single-ended	Output	Termination	Table
--------------	--------	-------------	-------

		Rs Value		
		(for each load)		
Output	Loads	Zo = 50Ω	Zo =60Ω	
PCI/USB	1	36	43	
PCI/USB	2	22	33	
REF	1	39	47	
REF	2	27	36	
REF	3	10	20	

Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V _{IL}		GND-0.5			V	1
Input High Voltage	V _{IH}	Except for SMBus interface			V _{DD} +0.5V	V	1
Input High Voltage	VIHSMB	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Case Temperature	Тс				110	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

¹Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

DC Electrical Characteristics - Differential Current Mode Outputs

 $T_A = T_{COM}$; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	1	2.4	4	V/ns	1, 2, 3
Slew rate matching	∆dV/dt	Slew rate matching, Scope averaging on		9	20	%	1, 2, 4
Rise/Fall Time Matching	∆Trf	Rise/fall matching, Scope averaging off			125	ps	1, 8, 9
Voltage High	VHigh	Statistical measurement on single-ended signal using	660	772	850	mV	1
Voltage Low	VLow	oscilloscope math function. (Scope averaging on)	-150	9	150	ni v	1
Max Voltage	Vmax	Measurement on single ended		810	1150	mV	1, 7
Min Voltage	Vmin	signal using absolute value.	-300	-17		111.V	1, 7
Vswing	Vswing	Scope averaging off	300	1446		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	351	550	mV	1, 5
Crossing Voltage (var)	∆-Vcross	Scope averaging off		24	140	mV	1, 6

¹Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/($3xR_R$). For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32mA$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7V @ Z_O = 50\Omega$ (100 Ω differential impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

⁷ Includes overshoot and undershoot.

⁸ Measured from single-ended waveform

⁹ Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics - Input/Supply/Common Parameters

$TA = T_{COM}$	Supply	Voltage	VDD = 3.3	V +/-5%
$1 1 1 = 1 \mathbf{C} 0 \mathbf{W}$	Cuppiy	vonugo	100 - 0.0	V 17 070

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	Т _{сом}	Commmercial range	0		70	°C	1
Input High Voltage	V _{IH}	Single-ended inputs, except SMBus, low threshold and tri- level inputs	2		V _{DD} + 0.3	V	1
Input Low Voltage	V _{IL}	Single-ended inputs, except SMBus, low threshold and tri- level inputs	GND - 0.3		0.8	V	1
	I _{IN}	Single-ended inputs, $V_{IN} = GND, V_{IN} = VDD$	-5		5	uA	1
Input Current	I _{INP}	Single-ended inputs. V _{IN} = 0 V; Inputs with internal pull up resistors V _{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Low Threshold Input- High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V _{DD} + 0.3	V	1
Low Threshold Input- Low Voltage	V_{IL_FS}	3.3 V +/-5%	V _{SS} - 0.3		0.35	V	1
Input Frequency	F _i			25.00		MHz	2
Pin Inductance	L _{p in}				7	nH	1
	C _{IN}	Logic Inputs			5	pF	1
Capacitance	C _{OUT}	Output pin capacitance			5	рF	1
	CINX	X1 & X2 pins			5	рF	1
Clk Stabilization	Τ _{stab}	From V _{DD} Power-Up and after input clock stabilization or de- assertion of PD# to 1st clock			1.8	ms	1,2
SS Modulation Frequency	f _{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz	1
Tdrive_PD#	t _{drvpd}	Differential output enable after PD# de-assertion		200.000	300	us	1,3
Tfall	t _F	Fall time of control inputs			5	ns	1,2
Trise	t _R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V _{ILSMB}				0.8	V	1
SMBus Input High Voltage	V _{IHSMB}		2.1		V _{DDSMB}	V	1
SMBus Output Low Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	1
SMBus Sink Current	IPULLUP	@ V _{OL}	4			mA	1
Nominal Bus Voltage	V _{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t _{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t _{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f _{maxsmb}	Maximum SMBus operating frequency			100	kHz	1

¹Guaranteed by design and characterization, not 100% tested in production.

 $^2\mbox{Control}$ input must be monotonic from 20% to 80% of input swing.

 3 Time from deassertion until outputs are >200 mV

IDT® PCIE GEN 2/3 & QPI CLOCK FOR ROMLEY-BASED SERVERS

AC Electrical Characteristics - Differential Current Mode Outputs

	had = 1/DD = 2.2 M + 1/E9/
$IA = I_{COM}$; Supply VOI	tage VDD = 3.3 V +/-5%

in ioom, eappij renage							
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t _{DC}	Measured differentially, PLL Mode	45	50.1	55	%	1
Skew, Output to Output	t _{sk3 SRC}	Across all SRC outputs, V _T = 50%		13.5	50	ps	1
Skew, Output to Output	t _{sk3CPU}	Across all CPU outputs, V _T = 50%		43	50	ps	1
Jitter, Cycle to cycle t	CPU, SRC, NS_SAS outputs		35	50	ps	1,3	
unier, Oyele to eyele	t _{jcyc-cyc}	DOT96 output		75	250	ps	1,3

¹Guaranteed by design and characterization, not 100% tested in production.

 2 I_{REF} = V_{DD}/(3xR_R). For R_R = 475 Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50 Ω .

³ Measured from differential waveform

Electrical Characteristics - Phase Jitter Parameters

 T_A = 0 - 70°C; Supply Voltage $V_{DD/}V_{DDA}$ = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
	t _{iphPCleG1}	PCIe Gen 1		28	86	ps (p-p)	1,2,3,6
		PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.9	3	ps (rms)	1,2,6
	t _{jphPCleG2} t _{jphPCleG3}	PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.7	3.1	ps (rms)	1,2,6
		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.4	1	ps (rms)	1,2,4,6
Phase Jitter		QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.15	0.5	ps (rms)	1,5,7
	t _{jphQPI_SMI}	QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.13	0.3	ps (rms)	1,5,7
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.11	0.2	ps (rms)	1,5,7
	t _{jphSAS12G}	SAS12G (Filtered REFCLK Jitter 20KHz to 20MHz.)		0.34	0.4	ps (rms)	1,8,9
	t _{jphSAS12G}	SAS 12G		0.70	1.3	ps (rms)	1,5,8

¹ Guaranteed by design and characterization, not 100% tested in production.

² See http://www.pcisig.com for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

⁶ Applied to SRC outputs

⁷ Applies to CPU outputs

⁸ Applies to NS_SAS, NS_SRC outputs, Spread Off

⁹ Intel calculation from raw phase noise data

Electrical Characteristics - PCI

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R _{DSP}	$V_{O} = V_{DD}^{*}(0.5)$	12		55	Ω	1
Output High Voltage	V _{он}	I _{он} = -1 mА	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current		MIN @V _{OH} = 1.0 V	-33			mA	1
Output High Current	I _{он}	MAX @V _{OH} = 3.135 V			-33	mA	1
		MIN @V _{OL} = 1.95 V	30			mA	1
Output Low Current	I _{OL}	MAX @ $V_{OL} = 0.4 V$			38	mA	1
Clock High Time	T _{HIGH}	1.5V	12			ns	1
Clock Low Time	T _{LOW}	1.5V	12			ns	1
Edge Rate	t _{sle wr/f}	Rising/Falling edge rate	1	1.8	4	V/ns	1,2
Duty Cycle	d _{t1}	$V_{T} = 1.5 V$	45	50.5	55	%	1
Group Skew	t _{skew}	$V_{T} = 1.5 V$		294	500	ps	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	$V_{T} = 1.5 V$		108	500	ps	1

 $T_A = 0 - 70^{\circ}C$; Supply Voltage $V_{DD/}V_{DDA} = 3.3 V + -5\%$,

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured between 0.8V and 2.0V

Electrical Characteristics - 48MHz

 $T_A = 0 - 70^{\circ}C$; Supply Voltage $V_{DD/}V_{DDA} = 3.3 V + -5\%$,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R _{DSP}	$V_{O} = V_{DD}^{*}(0.5)$	20		60	Ω	1
Output High Voltage	V _{он}	I _{ОН} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA			0.55	V	1
Output High Current	1	MIN @V _{OH} = 1.0 V	-29			mA	1
Output High Current	I _{он}	MAX @V _{OH} = 3.135 V			-33	mA	1
Output Low Current		MIN @V _{OL} = 1.95 V	29			mA	1
	I _{OL}	MAX @ $V_{OL} = 0.4 V$			27	mA	1
Clock High Time	T _{HIGH}	1.5V	8.094		10.036	ns	1
Clock Low Time	T _{LOW}	1.5V	7.694		9.836	ns	1
Edge Rate	t _{slewr/f_USB}	Rising/Falling edge rate	1	1.5	2	V/ns	1,2
Duty Cycle	d _{t1}	$V_{T} = 1.5 V$	45	51	55	%	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	V _T = 1.5 V		109	350	ps	1

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured between 0.8V and 2.0V

Electrical Characteristics - Current Consumption

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I _{DD3.30P}	All outputs active @100MHz, C_L = Full load;		380	400	mA	1
Powerdown Current	I _{DD3.3PDZ}	All differential pairs tri-stated		16	20	mA	1

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - REF

$T_A = 0 - 70^{\circ}C$; Supply Voltage \	$V_{DD}/V_{DDA} = 3.3 \text{ V} + -5\%$
--	---

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Output Impedance	R _{DSP}	$V_{O} = V_{DD}^{*}(0.5)$	12		55	Ω	1
Output High Voltage	V _{OH}	I _{ОН} = -1 mA	2.4			V	1
Output Low Voltage	V _{OL}	$I_{OL} = 1 \text{ mA}$			0.55	V	1
Output High Current		MIN @V _{OH} = 1.0 V	-33			mA	1
	I _{ОН}	MAX @V _{OH} = 3.135 V			-33	mA	1
Output Low Current		MIN @V _{OL} = 1.95 V	30			mA	1
	I _{OL}	MAX @ $V_{OL} = 0.4 V$			38	mA	1
Clock High Time	T _{HIGH}	1.5V	27.5			ns	1
Clock Low Time	T _{LOW}	1.5V	27.5			ns	1
Edge Rate	t _{sle wr/f}	Rising/Falling edge rate	1	1.9	4	V/ns	1,2
Duty Cycle	d _{t1}	V _T = 1.5 V	45	50.5	55	%	1
Jitter, Cycle to cycle	t _{jcyc-cyc}	V _T = 1.5 V		75	1000	ps	1

See "Single-ended Test Loads Page" for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured between 0.8V and 2.0V

Clock AC Tolerances

	CPU	SRC, NS_SAS, NS_SRC	PCI	DOT96	48MHz	REF	
PPM tolerance	100	100	100	100	100	100	ppm
Cycle to Cycle Jitter	50	50	500	250	350	1000	ps
Spread	-0.50%	-0.50%	-0.50%	0	0.00%	0.00%	%

Clock Periods – Outputs with Spread Spectrum Disabled

				Μ	easurement Wi	ndow				
	Center	1 Clock	1 us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC ON	Freq. MHz	-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max	Units	Notes
CPU	100.00000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
CFU	133.33333	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2
SRC, NS_SAS, NS_SRC	100.00000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
PCI	33.33333	29.49700		29.99700	30.00000	30.00300		30.50300	ns	1,2
DOT96	96.00000	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2
48MHz	48.00000	20.48125		20.83125	20.83333	20.83542		21.18542	ns	1,2
REF	14.31818	69.78429		69.83429	69.84128	69.84826		69.89826	ns	1,2

Clock Periods – Outputs with Spread Spectrum Enabled

				M	easurement Wi	ndow				
	Center	1 Clock	1 us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC ON	Freq. MHz	-c2cjitter AbsPer Min	-SSC Short-Term Average	- ppm Long-Term Average	0 ppm Period Nominal	Average	+SSC Short-Term Average	+c2c jitter AbsPer Max	Units	Notes
	00.75	0.0.4000	Min	Min	10.00500	Max	Max	10 10 107		10
CPU	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2
010	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2
PCI	33.25	29.49718	29.99718	30.07218	30.07519	30.07820	30.15320	30.65320	ns	1,2
SRC	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2

 $^1\mbox{Guaranteed}$ by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- · Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

How to Read

- · Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- · Controller (host) will send a separate start bit
- · Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if X_(H) was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

		Index Block F	Read O	1
	Co	ntroller (Host)		IDT (Slave/Receiver)
	Т	starT bit		
	S	lave Address		
	WR	WRite		
				ACK
	Beg	inning Byte = N		
			-	ACK
	RT	Repeat starT		
Slave Address				
	RD	ReaD		
				ACK
				Data Byte Count=X
		ACK		
				Beginning Byte N
		ACK		
			e	0
		0	X Byte	0
		0	×	0
		0		
			1	Byte N + X - 1
	Ν	Not acknowledge		
	Р	stoP bit		

Index Block Write Operation Controller (Host) IDT (Slave/Receiver) Т starT bit Slave Address WR WRite ACK Beginning Byte = N ACK Data Byte Count = X ACK Beginning Byte N ACK 0 \times Byte 0 0 0 0 0 Byte N + X - 1 ACK Ρ stoP bit

SMBus write address = D2 hex

SMBus read address = D3 hex

SMBus Table: Output Enable Register

Byte 0	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	24/25	DOT96 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 6	50/49	NS_SAS1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 5	48/47	NS_SAS0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 4	44/43	NS_SRC1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	42/41	NS_SRC0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 2	36/35	SRC2 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	34/33	SRC1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0	30/31	SRC0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1

SMBus Table: Output Enable Register

Byte	e 1 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	5	REF14_3x Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 6			RESERVED				0
Bit 5			RESERVED				0
Bit 4	62/61	CPU3	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	60/59	CPU2	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 2	56/55	CPU1	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	54/53	CPU0	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0	CPU/SRC/ PCI	Spread Spectrum Enable	Spread Off/On	RW	Spread Off	Spread On	0

SMBus Table: Output Enable Register

Byte	e 2 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7			RESERVED				0
Bit 6			RESERVED				0
Bit 5	13	PCI4 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 4	14	PCI3 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 3	15	PCI2 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 2	16	PCI1 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 1	17	PCI0 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 0	21	48MHz Enable	Output Enable	RW	Disable-Low	Enable	1

SMBus Table: Reserved

Byte 3	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7			RESERVED				0
Bit 6			RESERVED				0
Bit 5			RESERVED				0
Bit 4			RESERVED				0
Bit 3			RESERVED				0
Bit 2			RESERVED				0
Bit 1			RESERVED				0
Bit 0			RESERVED				0

SMBus Table: Reserved

Byte	e 4	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7				RESERVED				0
Bit 6				RESERVED				0
Bit 5				RESERVED				0
Bit 4				RESERVED				0
Bit 3				RESERVED				0
Bit 2				RESERVED				0
Bit 1				RESERVED				0
Bit 0				RESERVED				0

SMBus Table: Reserved

Byte	95 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7			RESERVED				0
Bit 6			RESERVED				0
Bit 5			RESERVED				0
Bit 4	-	FS4	Freq. Sel 4	RW			0
Bit 3	-	FS3	Freq. Sel 3	RW	Soo NS S		1
Bit 2	-	FS2	Freq. Sel 2	RW	See NS_SAS/NS_SRC Frequency Table.		1
Bit 1	-	FS1	Freq. Sel 1	RW			1
Bit 0	-	FS0	Freq. Sel 0	RW		1	

SMB us Table: Test Mode and CPU/SRC/PCI Frequency Select Register

Byte	e 6 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-	Test Mode	Test Mode Type	RW	Hi-Z	REF/N	0
Bit 6	-	Test Select	Select Test Mode	RW	Disable	Enable	0
Bit 5	-		RESERVED				0
Bit 4	-	100M_133M# (See note)	Frequency Select	R	133MHz	100MHz	Latch
Bit 3	-	FS3	Freq. Sel 3	RW			1
Bit 2	-	FS2	Freq. Sel 2	RW	See CPU/SRC/	PCI Frequency	0
Bit 1	-	FS1	Freq. Sel 1	RW	Select	Table	0
Bit 0	-	FS0	Freq. Sel 0	RW			0

Note: Internal Pull up on 100M_133M# pin will result in default CPU frequency of 100 MHz.

SMBus Table: Vendor & Revision ID Register

Byte 7	7 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-	RID3		R	R		0
Bit 6	-	RID2	REVISION ID	R	0011 fe	0	
Bit 5	-	RID1	REVISIONID	R	001110	1	
Bit 4	-	RID0		R		1	
Bit 3	-	VID3		R			0
Bit 2	-	VID2	VENDOR ID	R	0001 for	· ICS/IDT	0
Bit 1	-	VID 1	VENDORID	R	000110	105/101	0
Bit 0	-	VID0		R			1

SMBus Table: Byte Count Register

Byte	8 Pin #	Name	Control Function	Туре	0	1	Default
Bit 7	-	BC7		RW			0
Bit 6	-	BC6		RW	Writing to thi	s register will	0
Bit 5	-	BC5		RW	0	many bytes will	0
Bit 4	-	BC4	Byte Count	RW	be read bac	0	
Bit 3	-	BC3	Programming b(7:0)	RW		1	
Bit 2	-	BC2		RW	by	0	
Bit 1	-	BC1]	RW	(0 to 9		1
Bit 0	-	BC0		RW			0

SMBus Table: Device ID Register

Byte 9	Pin # Name		Control Function		0	1	Default
Bit 7		DID7		R	-	-	0
Bit 6		DID6		R	-	-	0
Bit 5		DID5		R	-	-	0
Bit 4		DID4	Device ID	R	-	-	1
Bit 3		DID3	(17 hex)	R	-	-	0
Bit 2		DID2		R	-	-	1
Bit 1		DID1		R	-	-	1
Bit 0		DID0		R	-	-	1

IDT® PCIE GEN 2/3 & QPI CLOCK FOR ROMLEY-BASED SERVERS

17

Line	Byte 1, Bit 0 Spread Enable	Byte6 Bit3 FS3	Byte6 Bit2 FS2	Byte6 Bit1 FS1	Byte6 Bit0 FS0	CPU Speed for 100MHz	CPU Speed for 133MHz	SRC (MHz)	PCI (MHz)	Spread %
0	0	0	0	0	0	89.97	119.97	89.97	29.99	
1	0	0	0	0	1	91.28	121.70	91.28	30.43	
2	0	0	0	1	0	92.58	123.44	92.58	30.86	
3	0	0	0	1	1	93.75	125.00	93.75	31.25	
4	0	0	1	0	0	95.05	126.73	95.05	31.68	
5	0	0	1	0	1	96.22	128.30	96.22	32.07	
6	0	0	1	1	0	97.53	130.03	97.53	32.51	
7	0	0	1	1	1	98.83	131.77	98.83	32.94	0%
8	0	1	0	0	0	100.00	133.33	100.00	33.33	0 /0
9	0	1	0	0	1	101.30	135.07	101.30	33.77	
10	0	1	0	1	0	102.47	136.63	102.47	34.16	
11	0	1	0	1	1	103.78	138.37	103.78	34.59	
12	0	1	1	0	0	105.08	140.10	105.08	35.03	
13	0	1	1	0	1	106.25	141.67	106.25	35.42	
14	0	1	1	1	0	107.55	143.40	107.55	35.85	
15	0	1	1	1	1	110.03	146.70	110.03	36.68	
16	1	0	0	0	0	89.97	119.97	89.97	29.99	
17	1	0	0	0	1	91.28	121.70	91.28	30.43	
18	1	0	0	1	0	92.58	123.44	92.58	30.86	
19	1	0	0	1	1	93.75	125.00	93.75	31.25	
20	1	0	1	0	0	95.05	126.73	95.05	31.68	
21	1	0	1	0	1	96.22	128.30	96.22	32.07	
22	1	0	1	1	0	97.53	130.03	97.53	32.51	
23	1	0	1	1	1	98.83	131.77	98.83	32.94	0.5%
24	1	1	0	0	0	100.00	133.33	100.00	33.33	-0.5%
25	1	1	0	0	1	101.30	135.07	101.30	33.77	
26	1	1	0	1	0	102.47	136.63	102.47	34.16	
27	1	1	0	1	1	103.78	138.37	103.78	34.59	
28	1	1	1	0	0	105.08	140.10	105.08	35.03	
29	1	1	1	0	1	106.25	141.67	106.25	35.42	
30	1	1	1	1	0	107.55	143.40	107.55	35.85	
31	1	1	1	1	1	110.03	146.70	110.03	36.68	

CPU/SRC/PCI Frequency Selection Table

	Byte5 Bit4	Byte5 Bit3	Byte5 Bit2	Byte5 Bit1	Byte5 Bit0	NS_xxx
Line	FS4	FS3	FS2	FS1	FS0	(MHz)
0	0	0	0	0	0	58.33
1	0	0	0	0	1	61.11
2	0	0	0	1	0	63.89
3	0	0	0	1	1	66.67
4	0	0	1	0	0	69.44
5	0	0	1	0	1	72.22
6	0	0	1	1	0	75.00
7	0	0	1	1	1	77.78
8	0	1	0	0	0	80.56
9	0	1	0	0	1	83.33
10	0	1	0	1	0	86.11
11	0	1	0	1	1	88.89
12	0	1	1	0	0	91.67
13	0	1	1	0	1	94.44
14	0	1	1	1	0	97.22
15	0	1	1	1	1	100.00
16	1	0	0	0	0	102.78
17	1	0	0	0	1	105.56
18	1	0	0	1	0	108.33
19	1	0	0	1	1	111.11
20	1	0	1	0	0	113.89
21	1	0	1	0	1	116.67
22	1	0	1	1	0	119.44
23	1	0	1	1	1	122.22
24	1	1	0	0	0	125.00
25	1	1	0	0	1	127.78
26	1	1	0	1	0	130.56
27	1	1	0	1	1	133.33
28	1	1	1	0	0	136.11
29	1	1	1	0	1	138.89
30	1	1	1	1	0	141.67
31	1	1	1	1	1	144.44

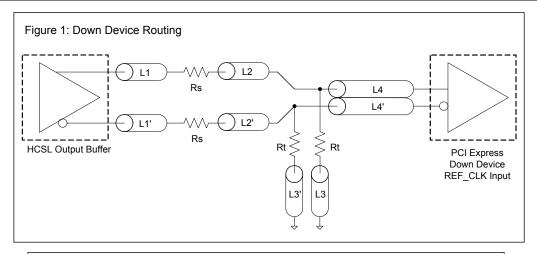
NS_SAS Margining Table

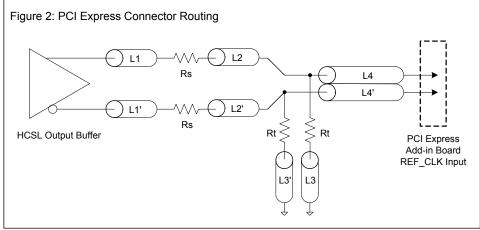
NOTE: Operation at other than the default entry is not guaranteed. These values are for margining purposes only.

DIF Reference Cloc	K Contraction of the second seco		
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 1000hm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 1000hm differential trace	0.225 min to 12.6 max	inch	2

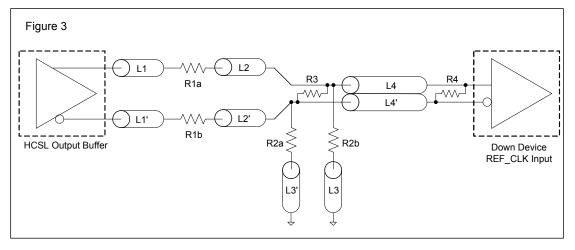




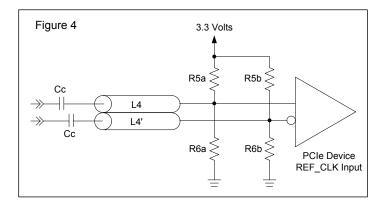
	Alternative Termination for LVDS and other Common Differential Signals (figure 3)								
Vdiff Vp-p Vcm R1 R2 R3 R4 Note							Note		
0.45v	0.22v	1.08	33	150	100	100			
0.58	0.28	0.6	33	78.7	137	100			
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible		
0.60	0.3	1.2	33	174	140	100	Standard LVDS		

R1a = R1b = R1

R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)							
Component	Value	Note					
R5a, R5b	8.2K 5%						
R6a, R6b	1K 5%						
Сс	0.1 µF						
Vcm	0.350 volts						



Test Clarification Table

Comments	F	IW	S	W	
	TEST_SEL HW PIN	TEST_MODE HW PIN	TE ST ENTRY BIT B6b6	REF/N or HI-Z B6b7	OUTPUT
	0	Х	0	Х	NORMAL
Power-up w/ TEST_SEL = 1 (>2.0V) to enter test mode.	1	0	Х	0	HI-Z
Cycle power to disable test mode.	1	0	Х	1	REF/N
	1	1	Х	0	REF/N
	1	1	Х	1	REF/N
If TEST_SEL HW pin is 0 during power-up,	0	Х	1	0	HI-Z
test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N. TEST_Mode pin is not used. Cycle power to disable test mode.	0	х	1	1	REF/N

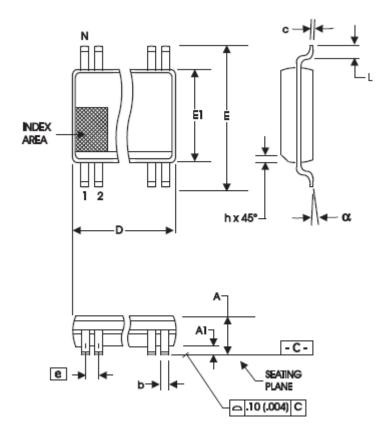
B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B6b7: 1= REF/N, Default = 0 (HI-Z)

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Thermal Resistance Junction to	θ_{JA}	Still air		68.2		° C/W
Ambient	θ_{JA}	1 m/s air flow		63.3		° C/W
	θ_{JA}	2 m/s air flow		59.6		° C/W
Thermal Resistance Junction to Case	θ _{JC}			32.5		° C/W
Thermal Resistance Junction to Board	θ_{JB}			51.5		° C/W

Package Outline and Package Dimensions (64-pin TSSOP)



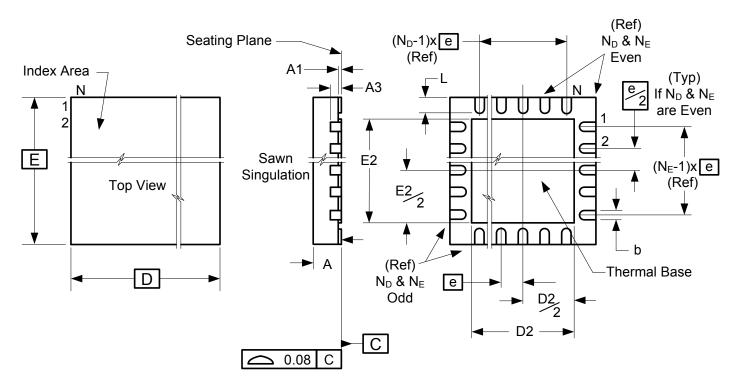
	(240 mil)	(20 mil)		
SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIO	
	MIN	MAX	MIN	MAX
A	-	1.20		.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
С	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
е	0.50 BASIC		0.020	BASIC
L	0.45		.018	.030
Ν	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa		0.10		.004

VARIATIONS

Ν	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039



Package Outline and Package Dimensions (64-pin MLF)

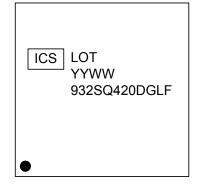
THERMALLY ENHANCED, VERY THIN, FINE PITCH QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIO	NS
N	64
ND	16
NE	16

SYMBOL	MIN.	MAX.	
A	0.8	1.0	
A1	0 0.05		
A3	0.25 Reference		
b	0.18	0.3	
е	0.50 BASIC		
D x E BASIC	9.00 x 9.00		
D2 MIN. / MAX.	6.00	6.25	
E2 MIN. / MAX.	6.00	6.25	
L MIN. / MAX.	0.30	0.50	

IDT® PCIE GEN 2/3 & QPI CLOCK FOR ROMLEY-BASED SERVERS

Marking Diagram (TSSOP)



Marking Diagram (MLF)



Notes:

- 1. 'LOT' denotes lot number.
- 2. 'YYWW' is the date code.
- 3. 'COO' denotes country of origin.
- 4. 'L' or 'LF' denotes RoHS compliant package.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
932SQ420DGLF	Tubes	64-pin TSSOP	0 to +70° C
932SQ420DGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C
932SQ420DKLF	Tray	64-pin MLF	0 to +70° C
932SQ420DKLFT	Tape and Reel	64-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

"D" is the device revision designator (will not correlate with the datasheet revision).

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

Rev.	Issue Date	Who	Description	Page #
0.9	9/16/2010	RDW	Initial Release	-
Α	9/20/2010	RDW	Minor typo corrections	Various
В	3/1/2011	RDW	Added rise/fall variation to DC Electrical Characteristics Table	9
С	3/9/2011	RDW	Corrected Line 0 of NS_SAS Margining Table.	19
D	4/28/2011	RDW	Corrected MLF packaging pin description. Pin 37 was missing.	7
			Updated Power Down Functionality table to clarify functionality of single-	
E	7/26/2011	RDW	ended outputs in power down.	2
			1. Added "Case Temperature" spec to Abs Max ratings	
F	9/20/2011	RDW	2. Added Thermal Characteristics	Various
			1. Updated Phase Jitter Table to correct typo in "Conditions" column for	11, 23,
G	12/8/2011	RDW	SAS.	24
			2. Mark Spec Added.	24
н	4/18/2012	אחם	1. Updated Rp values on Output Terminations Table from 43.2 ohms to	8
	4/10/2012		42.2 or 43.2 ohms to be consistent with Intel.	0

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015 408-284-8200 Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp pcclockhelp@idt.com

Corporate Headquarters

Integrated Device Technology, Inc. www.idt.com



© 2011 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice. IDT, ICS, and the IDT logo are trademarks of Integrated Device Technology, Inc. Accelerated Thinking is a service mark of Integrated Device Technology, Inc. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners. Printed in USA