Independent Multicell Battery Stack Fault Monitor

FEATURES

- **Monitors Up to 12 Li-Ion Cells in Series (60V Max)**
- **Stackable Architecture Enables >1000V Systems**
- **1% Maximum Overvoltage Detection Level Error**
- **Adjustable Overvoltage and Undervoltage Detection**
- **Self Test Features Guarantee Accuracy**
- **Robust Fault Detection Using Differential Signals**
- Simple Pin-Strapped Configuration Allows Battery Monitoring without a Microcontroller
- 15.5ms to Monitor All Cells in a System
- Programmable Response Time
- Two Temperature Monitor Inputs
- Low Power Idle Mode
- 36-Lead SSOP Package

APPLICATIONS

- Redundant Battery Monitor
- Hybrid Electric Vehicles
- Battery Backup Systems
- Power Systems Using Multiple Battery Cells

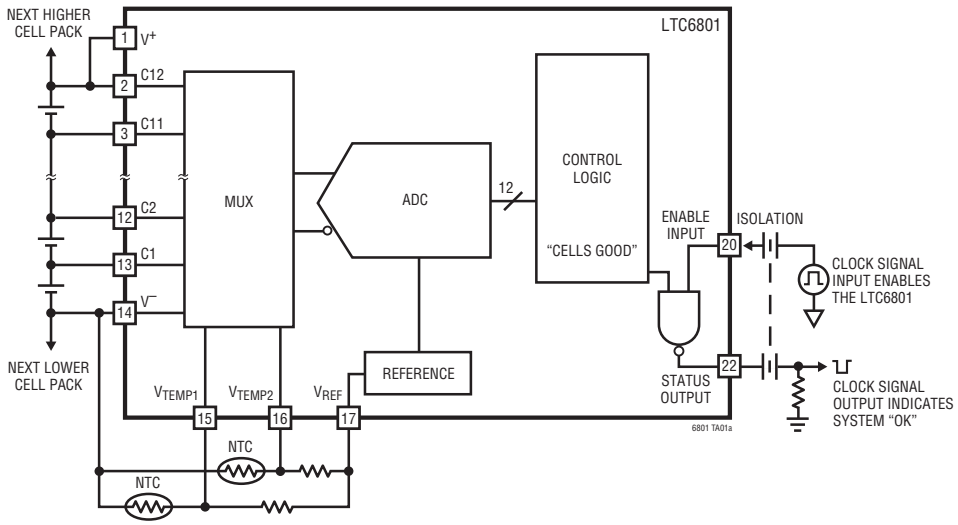
DESCRIPTION

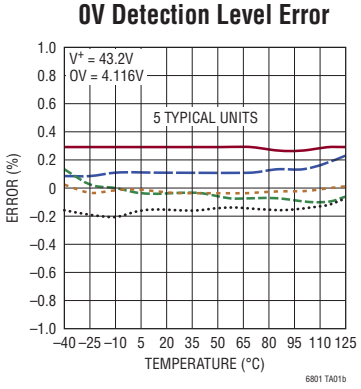
The LTC®6801 is a multicell battery monitoring IC incorporating a 12-bit ADC, a precision voltage reference, sampled comparator, and a high voltage input multiplexer. The LTC6801 can monitor as many as 12 series connected battery cells for overvoltage, undervoltage, and overtemperature conditions, indicating whether the cells are within specified parameters. The LTC6801 generates a clock output when no fault conditions exist. Differential clocking provides high noise immunity and ensures that battery stack fault conditions cannot be hidden by frozen bits or short circuit conditions.

Each LTC6801 can operate with a battery stack voltage up to 60V and multiple LTC6801 devices can be stacked to monitor each individual cell in a long battery string. When multiple devices are stacked, the status signal of each LTC6801 can be daisy-chained, without opto-couplers or isolators, providing a single status output for the entire battery string.

The LTC6801 is configurable by external pin strapping. Adjustable overvoltage and undervoltage thresholds support various Li-Ion chemistries. Selectable measurement times allow users to save power.

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 60V
Input Voltage (Relative to V^-)
- C1 ..... –0.3V to 9V
- C12 ..... V^+ –0.3V to V^+ + 0.3V
- All Other Pins (Not C Inputs) ..... –0.3V to 7V

Voltage Between Inputs
- Cn to Cn-1* ..... –0.3V to 9V
- C12 to C8 ..... –0.3V to 25V
- C8 to C4 ..... –0.3V to 25V
- C4 to V^- ..... –0.3V to 25V

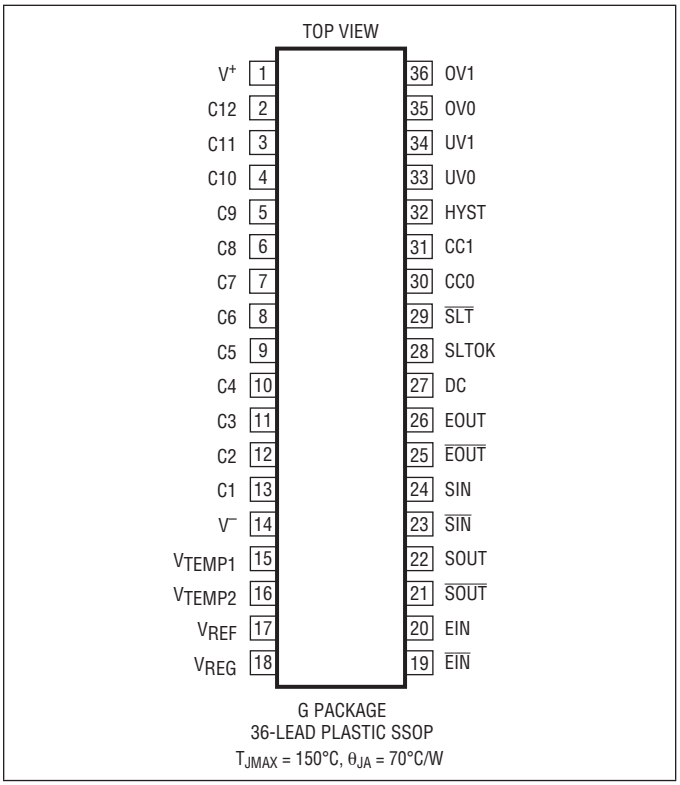
Operating Temperature Range
- LTC6801I ..... –40°C to 85°C
- LTC6801H ..... –40°C to 125°C

Specified Temperature Range
- LTC6801I ..... –40°C to 85°C
- LTC6801H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

*n = 2 to 12

PIN CONFIGURATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6801IG#PBF	LTC6801IG#TRPBF	LTC6801G	36-Lead Plastic SSOP	–40°C to 85°C
LTC6801HG#PBF	LTC6801HG#TRPBF	LTC6801G	36-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 43.2V, V^- = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Specifications							
V_{ERR}	Overvoltage (OV) or Undervoltage (UV) Detection Level Error	(Note 2)					
		2.106V ≤ V_{CELL} ≤ 4.498V		–0.8		0.8	%
		2.106V ≤ V_{CELL} ≤ 4.498V	●	–1		1	%
		1.531V ≤ V_{CELL} < 2.106V		–1		1	%
		1.531V ≤ V_{CELL} < 2.106V	●	–1.3		1.3	%
		V_{CELL} = 0.766V		–1.5		1.5	%
		V_{CELL} = 0.766V	●	–2		2	%
V_S	Supply Voltage, V^+ Relative to V^-	V_{ERR} Specifications Met	●	10		50	V
V_{CELL}	Cell Voltage Range	Full Scale Voltage Range			5		V
V_{CM}	Common Mode Voltage Range Measured Relative to V^-	V_{ERR} Specifications Met					
		Range of Inputs Cn, n = 3 to 11	●	1.8		5 • n	V
		Range of Input C2	●	1.2		10	V
		Range of Input C1	●	0		5	V
V_{TV}	Temperature Input Detection Level Error (Relative to V_{REF}/2)	10V < V^+ < 50V	●	–13		17	mV
HYS	UV/OV Detection Hysteresis Error (Relative to Selected Value)	10V < V^+ < 50V	●	–25		25	%
V_{REF}	Reference Pin Voltage	V_{REF} Pin Loaded With 100k to V^-		3.043	3.058	3.073	V
			●	3.038	3.058	3.078	V
	Reference Voltage Temperature Coefficient				8		ppm/°C
	Reference Voltage Hysteresis				50		ppm
	Reference Voltage Long Term Drift				60		ppm/$\sqrt{khr}$
V_{REG}	Regulator Pin Voltage	10V < V_S < 50V, No Load					
		LTC6801IG	●	4.5	5	5.5	V
		LTC6801HG	●	4.5	5	5.7	V
		10V < V_S < 50V, I_{LOAD} = 4mA					
		LTC6801IG	●	4.1	4.8		V
		LTC6801HG	●	4.1	4.8		V
	Regulator Pin Short Circuit Current Limit		●	5	9		mA
I_B	Input Bias Current	In/Out of Pins C1 Thru C12					
		When Measuring Cells During Self Test			100		µA
		When Measuring Cells	●	–10		10	µA
		When Idle			1		nA
I_M	Supply Current, Monitor Mode	Current Into the V^+ Pin While Monitoring for UV and OV Conditions, F_{ENA} = 10kHz					
		Continuous Monitoring		600	750	1000	µA
		Continuous Monitoring	●	500	750	1100	µA
		Monitor Every 130ms (Note 3)	●	110	200	320	µA
		Monitor Every 500ms (Note 3)	●	50	100	160	µA
I_{QS}	Supply Current, Idle	Current into the V^+ Pin When Idle, F_{ENA} = 0					
		LTC6801IG		23	30	42	µA
			●	20	30	45	µA
		LTC6801HG		23	30	42	µA
			●	20	30	48	µA
LTC6801 Timing Specifications							
T_{CYCLE}	Measurement Cycle Time	DC = CC1 = CC0 = V_{REG}	●	13	15.5	19	ms
F_{ENA}	Valid EIN/$\overline{EIN}$ Frequency		●	2		40	kHz
T_{ENA}	Valid EIN/$\overline{EIN}$ Period = 1/ F_{ENA}		●	25		500	µs
DC_{ENA}	Valid EIN/$\overline{EIN}$ Duty Cycle	F_{ENA} = 40kHz	●	40		60	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V^+ = 43.2V, V^- = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LTC6801 Single Ended Digital I/O Specifications ($\overline{SLT}$, SLTOK Pins)							
V_{IH}	Digital Input Voltage High	$\overline{SLT}$ Pin	●	2			V
V_{IL}	Digital Input Voltage Low	$\overline{SLT}$ Pin	●			0.5	V
V_{ODL}	Digital Output Voltage Low, Open Drain	$\overline{SLT}$ Pin, 10k to V_{REG}	●			0.3	V
V_{OH}	Digital Output Voltage High	SLTOK Pin, 10k to V^-	●	V_{REG} – 0.3			V
V_{OL}	Digital Output Voltage Low	SLTOK Pin, 10k to V_{REG}	●			0.3	V
I_{PU-ST}	Pull-Up Current	$\overline{SLT}$ Pin	●	2.5	5	10	µA
LTC6801 Differential Digital Input Specifications (SIN/$\overline{SIN}$, EIN/$\overline{EIN}$ Pins) (See Figure 1)							
V_{IDH}	Minimum Differential Input Voltage High	Differential Voltage Applied Between SIN and $\overline{SIN}$ or EIN and $\overline{EIN}$	●	1.7			V
V_{IDL}	Minimum Differential Input Voltage Low		●			–1.7	V
V_{IL}	Valid Input Voltage Low	Low Side of Differential Signal, Ref. to V^-	●	0		1.2	V
V_{IH}	Valid Input Voltage High	High Side of Differential Signal, Ref. to V^-	●	2.5		6	V
V_{DHYS}	Differential Input Hysteresis				1		V
V_{OPEN}	Open Circuit Voltage		●	2	2.5	3	V
R_{INCM}	Input Resistance, Common Mode		●	100	150		kΩ
R_{INDIFF}	Input Resistance, Differential	Between SIN to $\overline{SIN}$, EIN to $\overline{EIN}$	●	200	300		kΩ
LTC6801 Differential Digital Output Specifications (SOUT/$\overline{SOUT}$, EOUT/$\overline{EOUT}$ Pins)							
V_{ODH}	Digital Output Voltage High	Output Pins Loaded With 100k to V^-	●	V_{REG} – 0.4			V
V_{ODL}	Digital Output Voltage Low	Output Pins Loaded With 100k to V_{REG}	●			0.4	V
LTC6801 Three-Level Digital Input Specifications (OV0, OV1, UV0, UV1, HYST, DC, CC0 and CC1 Pins)							
V_{3IH}	Three-Level Digital Input Voltage High		●	V_{REG} – 0.3			V
V_{3IM}	Three-Level Digital Input Voltage Mid		●	V_{REF} – 0.3		V_{REF} + 0.3	V
V_{3IL}	Three-Level Digital Input Voltage Low		●			0.3	V
I_{PU}	Pull-Up Current	Pins DC, CC0, CC1, UV0 and UV1	●	0.5	1	2	µA
I_{PD}	Pull-Down Current	Pins HYST, OV0 and OV1	●	0.5	1	2	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: V_{CELL} refers to the voltage applied across the following pin combinations: Cn to Cn – 1 for n = 2 to 12, C1 to V^-.

Note 3: Guaranteed by continuous monitoring supply current specifications, not subject to test.

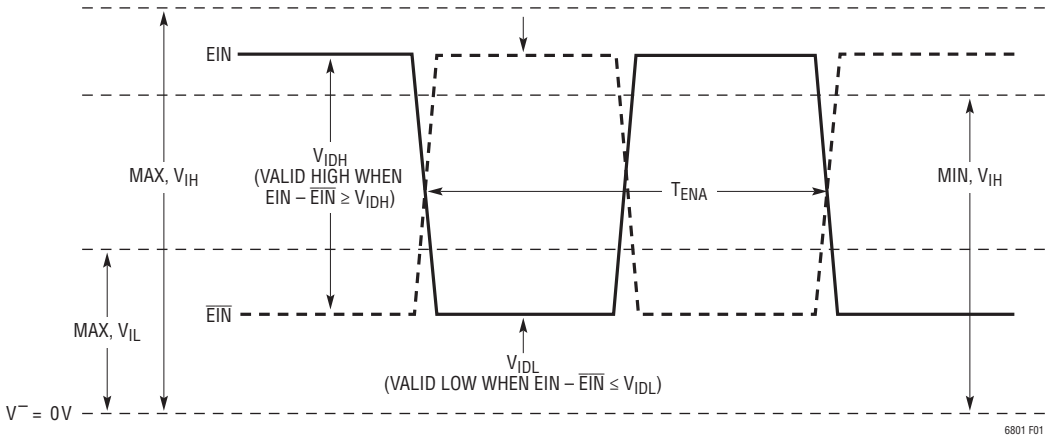
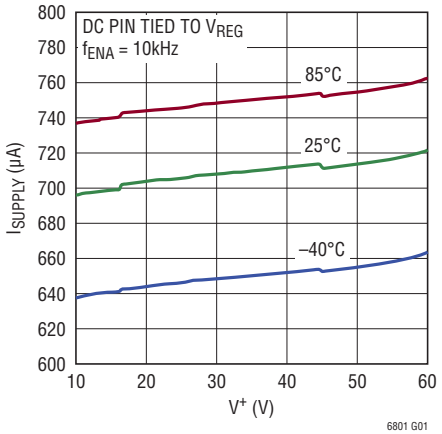


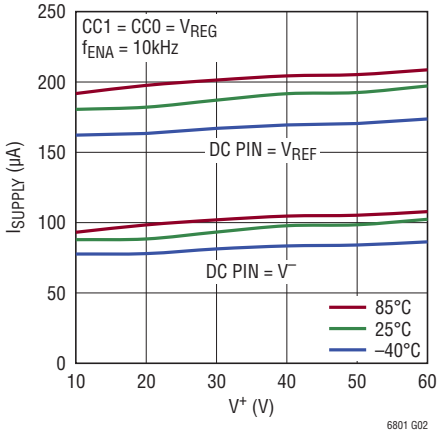
Figure 1. Differential Input Specifications

TYPICAL PERFORMANCE CHARACTERISTICS

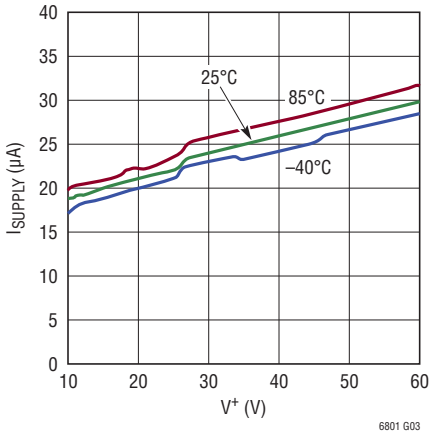
Supply Current, Monitor Mode



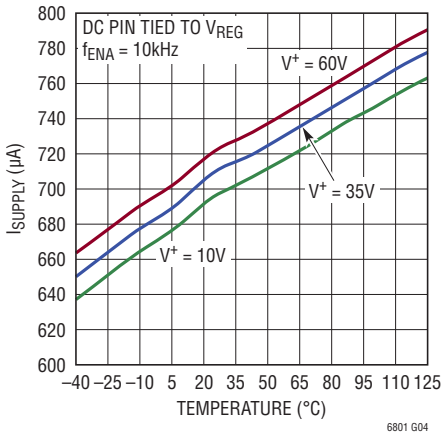
Supply Current, Monitor Mode



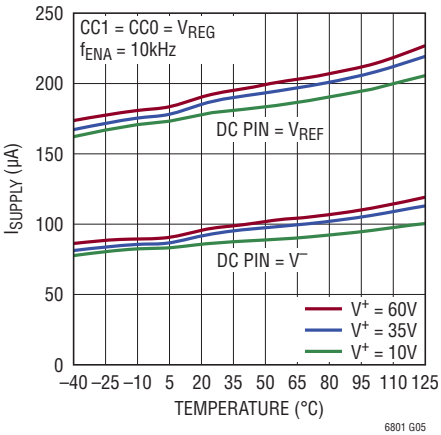
Supply Current, Idle Mode



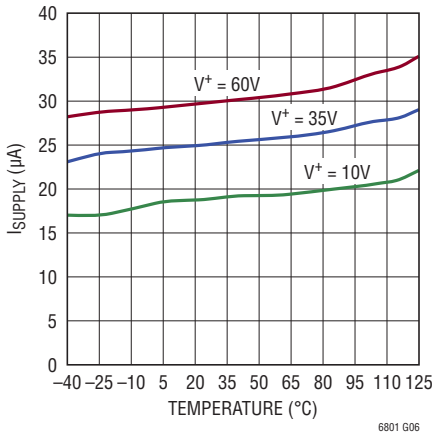
Supply Current, Monitor Mode



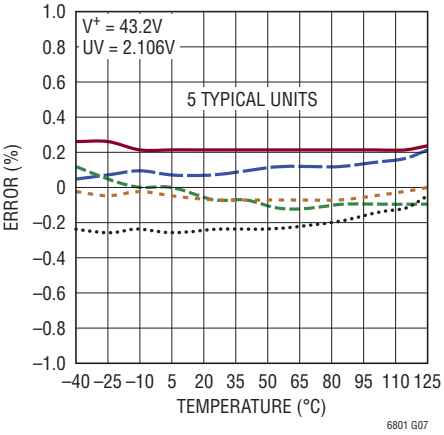
Supply Current, Monitor Mode



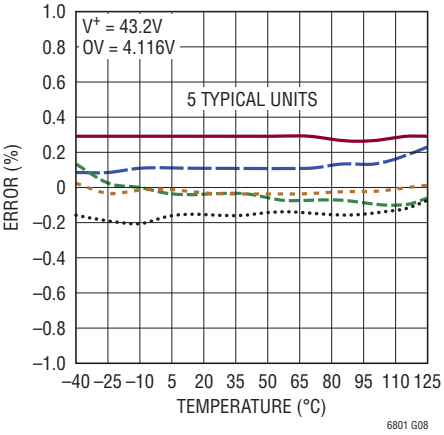
Supply Current, Idle Mode



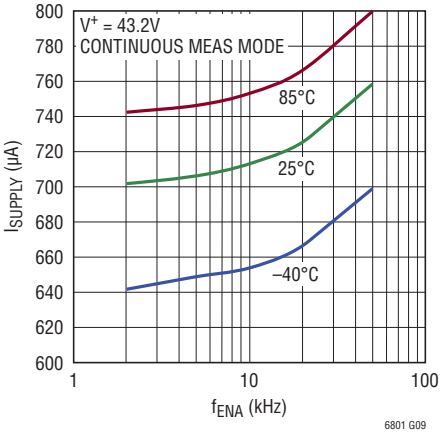
UV Detection Level Error



OV Detection Level Error

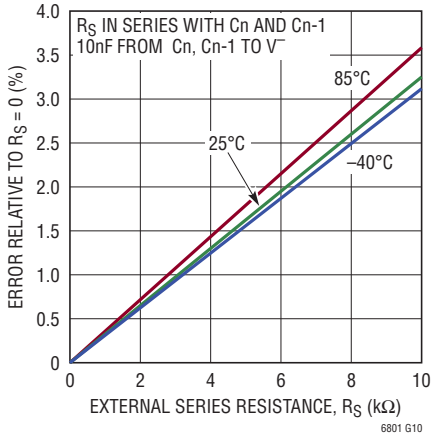


Supply Current

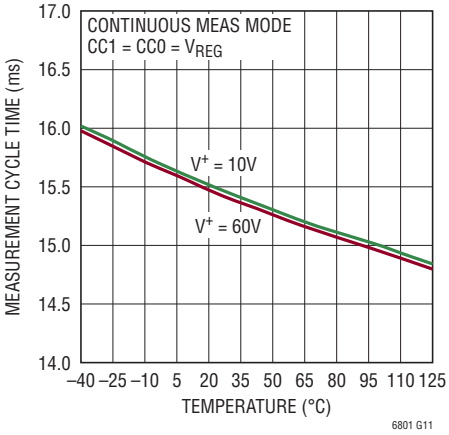


TYPICAL PERFORMANCE CHARACTERISTICS

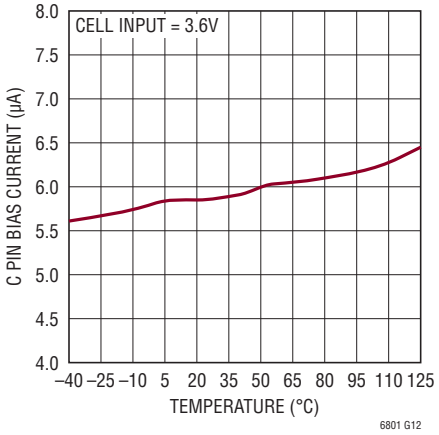
UV/OV Detection Level Error



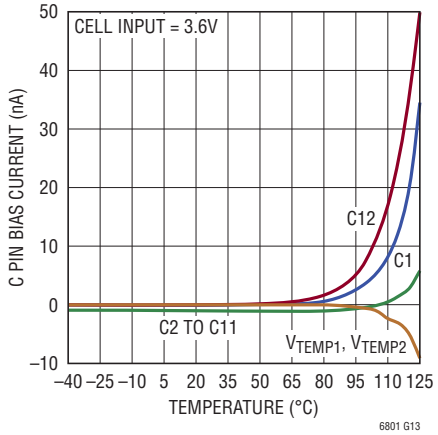
Measurement Cycle Time



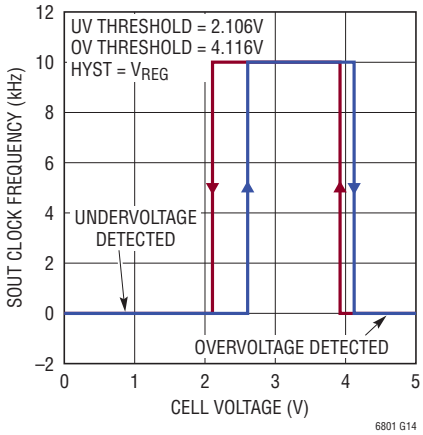
Cell Input Bias Current when Measuring



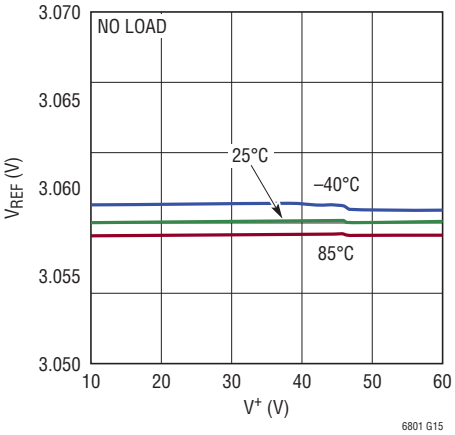
Cell Input Bias Current, Idle Mode



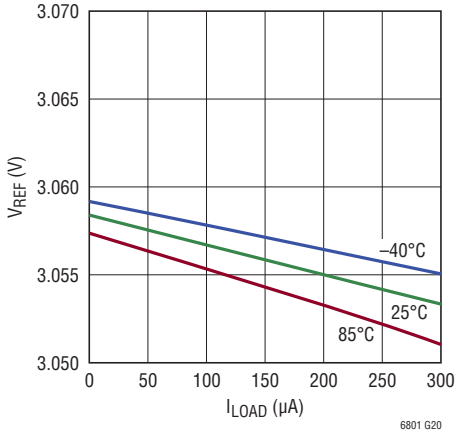
Cell Voltage Measurement Hysteresis



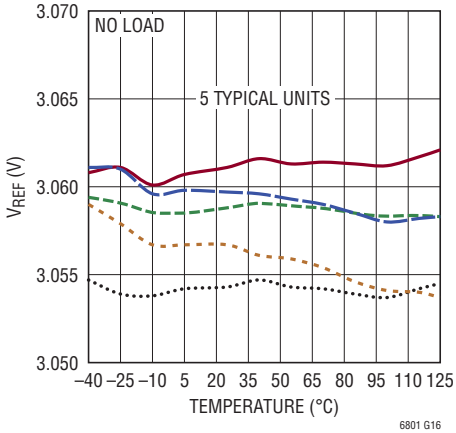
VREF Line Regulation



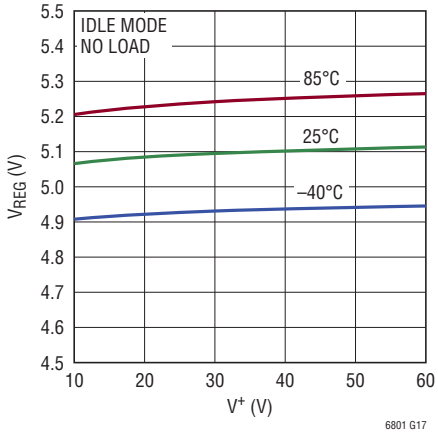
VREF Load Regulation



VREF Output Voltage

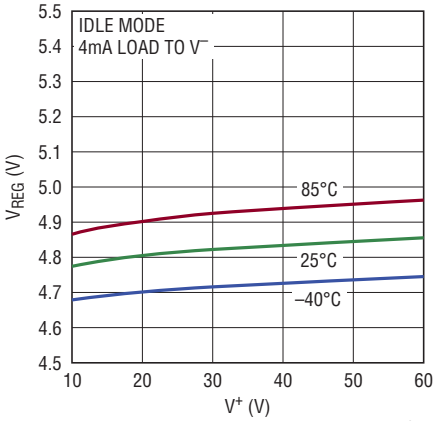


VREG Line Regulation

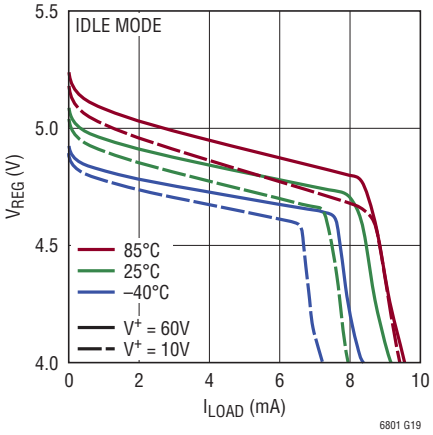


TYPICAL PERFORMANCE CHARACTERISTICS

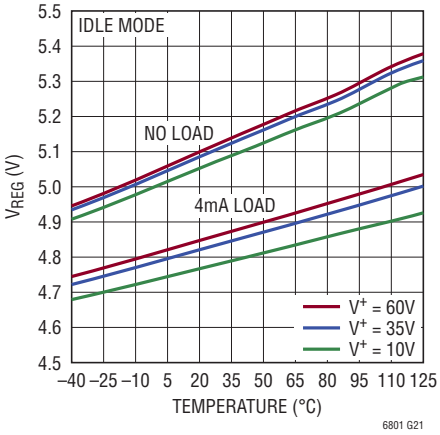
V_{REG} Line Regulation



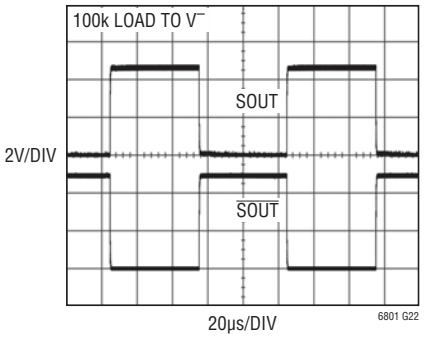
V_{REG} Load Regulation



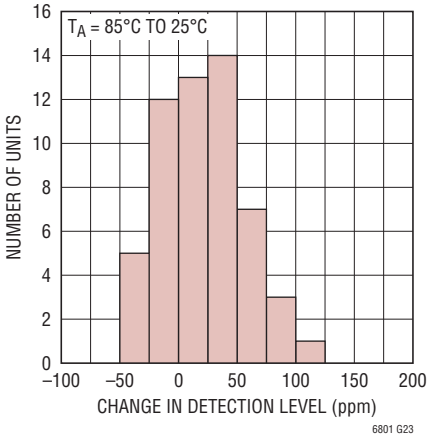
V_{REG} Output Voltage



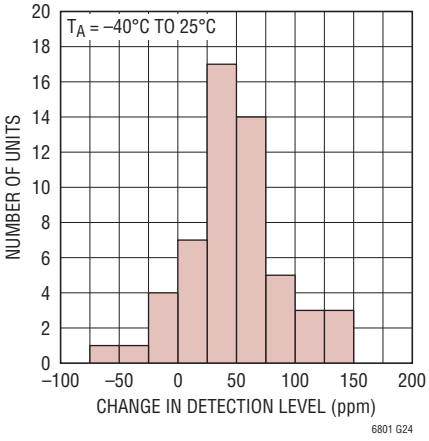
Status Output Operating at 10kHz



UV/OV Detection Level Thermal Hysteresis



UV/OV Detection Level Thermal Hysteresis



PIN FUNCTIONS

V^+ (Pin 1): Supply Voltage. Tied to the most positive potential in the battery stack. For example, the same potential as C12 when measuring a stack of 12 cells, or the same potential as C7 when measuring a stack of 7 cells.

C12, C11, ... C1 (Pin 2 to Pin 13): Cell Voltage Inputs. Up to 12 cells can be monitored. The lowest potential is tied to V^-. The next lowest potential is tied to C1 and so forth. Due to internal overvoltage protection, each C input must be tied to a potential equal to or greater than the next lower numbered C input. See the figures in the Applications Information section for more details on connecting batteries to the LTC6801. See Electrical Characteristics table for voltage range and input bias current requirements.

V^- (Pin 14): Tied to the most negative cell potential (bottom of monitored cell stack).

V_{TEMP1}, V_{TEMP2} (Pin 15, Pin 16): Temperature Sensor Inputs. The ADC will measure the voltages on V_{TEMP1} and V_{TEMP2} relative to V^-. The ADC measurements are referenced to the V_{REF} pin voltage. Therefore a simple thermistor and resistor combination connected to the V_{REF} pin can be used to monitor temperature. These pins have a fixed undervoltage threshold equal to one half V_{REF}. A filtering capacitor to V^- is recommended. Temperature sensor input pins may be tied to V_{REF} to disable.

V_{REF} (Pin 17): Reference Output, Nominally 3.058V. Requires a 1µF bypass capacitor to V^-. The V_{REF} pin can drive a 100k resistive load connected to V^-. V_{REF} must be buffered with an LT6003 amplifier, or similar device to drive heavier loads. V_{REF} becomes high impedance when the IC is disabled or idle between monitoring events.

V_{REG} (Pin 18): Regulator Output, Nominally 5V. Requires a 1µF bypass capacitor to V^-. The V_{REG} pin is capable of supplying up to 4mA to an external load and is continually enabled.

$\overline{EIN}$, EIN (Pin 19, Pin 20): Differential Enable Input. A clock signal greater than 2kHz will enable the LTC6801. For operation with a single-ended enable signal (up to 10kHz), drive EIN and connect a 1nF capacitor from $\overline{EIN}$ to V^-.

$\overline{SOUT}$, SOUT (Pin 21, Pin 22): Differential Status Output. Swings V^- to V_{REG}. This output will toggle at the same frequency as EIN/$\overline{EIN}$ when a valid signal is detected at SIN/$\overline{SIN}$ and the battery stack being monitored is within specified parameters, otherwise SOUT is low and $\overline{SOUT}$ high.

$\overline{SIN}$, SIN (Pin 23, Pin 24): Differential status input from the IC above. To indicate that the stack is good, SIN must be the same frequency and phase as EIN. See applications circuits for interfacing SIN to the SOUT above.

$\overline{EOUT}$, EOUT (Pin 25, Pin 26): A Buffered Version of EIN/$\overline{EIN}$. Swings V^- to V_{REG}. Must be capacitively coupled to the EIN/$\overline{EIN}$ inputs of the next higher voltage LTC6801 in a stack, or looped to SIN/$\overline{SIN}$ of the same chip (pins 23, 24).

DC (Pin 27): Duty Cycle Three-Level Input. This pin may be tied to V_{REG}, V_{REF} or V^-. The DC pin selects the duty cycle of the monitoring function and has an internal pull-up to V_{REG}. See Table 3.

SLTOK (Pin 28): Self Test Logic Output. SLTOK is held HIGH (V_{REG} voltage) upon reset or successful completion of a self test cycle. A LOW output level (V^- voltage) indicates the last self test cycle failed.

$\overline{SLT}$ (Pin 29): Self Test Open Collector Input/Output. $\overline{SLT}$ initiates a self test cycle when it is pulled low externally. When a high to low transition is detected, the next scheduled measurement cycle will be a self test cycle. $\overline{SLT}$ indicates a self test cycle is in progress when pulled low internally. A self test is automatically initiated after 1024 measurement cycles. This pin has an internal pull-up to V_{REG}.

CC0, CC1 (Pin 30, Pin 31): Cell Count Three-Level Inputs. These pins may be tied to V_{REG}, V_{REF} or V^-. CC1 and CC0 select the number of cells attached to the device and each pin has an internal pull-up to V_{REG}. See Table 5.

HYST (Pin 32): Hysteresis Three-Level Input. This pin may be tied to V_{REG}, V_{REF} or V^-. HYST selects the amount of hysteresis applied to the undervoltage and overvoltage threshold settings and has an internal pull-down to V^-. See Table 4.

PIN FUNCTIONS

UV0, UV1 (Pin 33, Pin 34): Undervoltage Three-Level Inputs. These pins may be tied to V_{REG}, V_{REF} or V^-. UV1 and UV0 select the undervoltage threshold and each pin has an internal pull-up to V_{REG}. See Table 2.

OV0, OV1 (Pin 35, Pin 36): Overvoltage Three-Level Inputs. These pins may be tied to V_{REG}, V_{REF} or V^-. OV1 and OV0 select the overvoltage threshold and each pin has an internal pull-down to V^-. See Table 1.

Table 1. Overvoltage Inputs

OV1	OV0	OVERVOLTAGE THRESHOLD (V)
V_{REG}	V_{REG}	4.498
V_{REG}	V_{REF}	4.403
V_{REG}	V^-	4.307
V_{REF}	V_{REG}	4.211
V_{REF}	V_{REF}	4.116
V_{REF}	V^-	4.020
V^-	V_{REG}	3.924
V^-	V_{REF}	3.828
V^-	V^-	3.733

Table 2. Undervoltage Inputs

UV1	UV0	UNDERVOLTAGE THRESHOLD (V)
V_{REG}	V_{REG}	2.871
V_{REG}	V_{REF}	2.680
V_{REG}	V^-	2.489
V_{REF}	V_{REG}	2.297
V_{REF}	V_{REF}	2.106
V_{REF}	V^-	1.914
V^-	V_{REG}	1.723
V^-	V_{REF}	1.531
V^-	V^-	0.766

Table 3. Duty Cycle Select

DC	NOMINAL CYCLE TIME*
V_{REG}	15.5ms
V_{REF}	Approximately 130ms
V^-	Approximately 500ms

*Cycle time based on LTC6801 measuring 12 cells and 2 temperatures.

Table 4. Hysteresis Select

HYST	UV HYSTERESIS*	OV HYSTERESIS
V_{REG}	500mV	200mV
V_{REF}	250mV	100mV
V^-	0mV	0mV

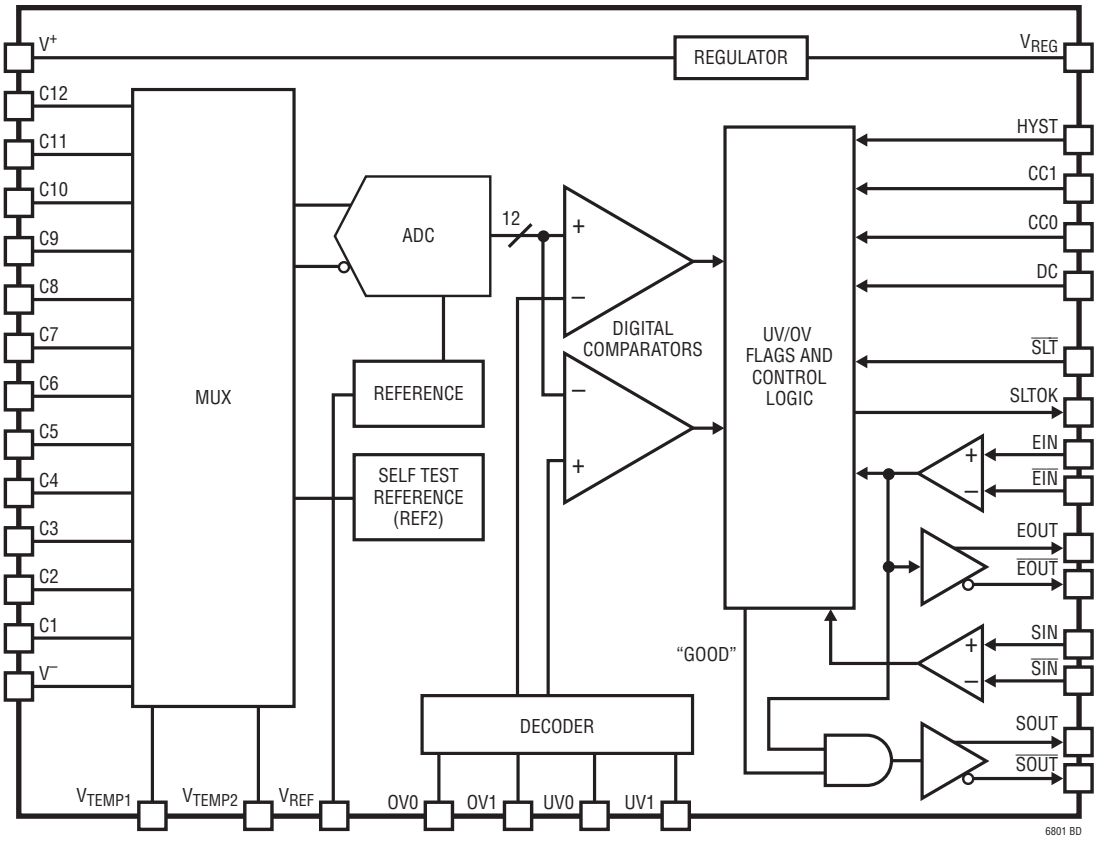
*UV hysteresis is disabled when the undervoltage threshold is set to 0.766V.

Table 5. Cell Count Select

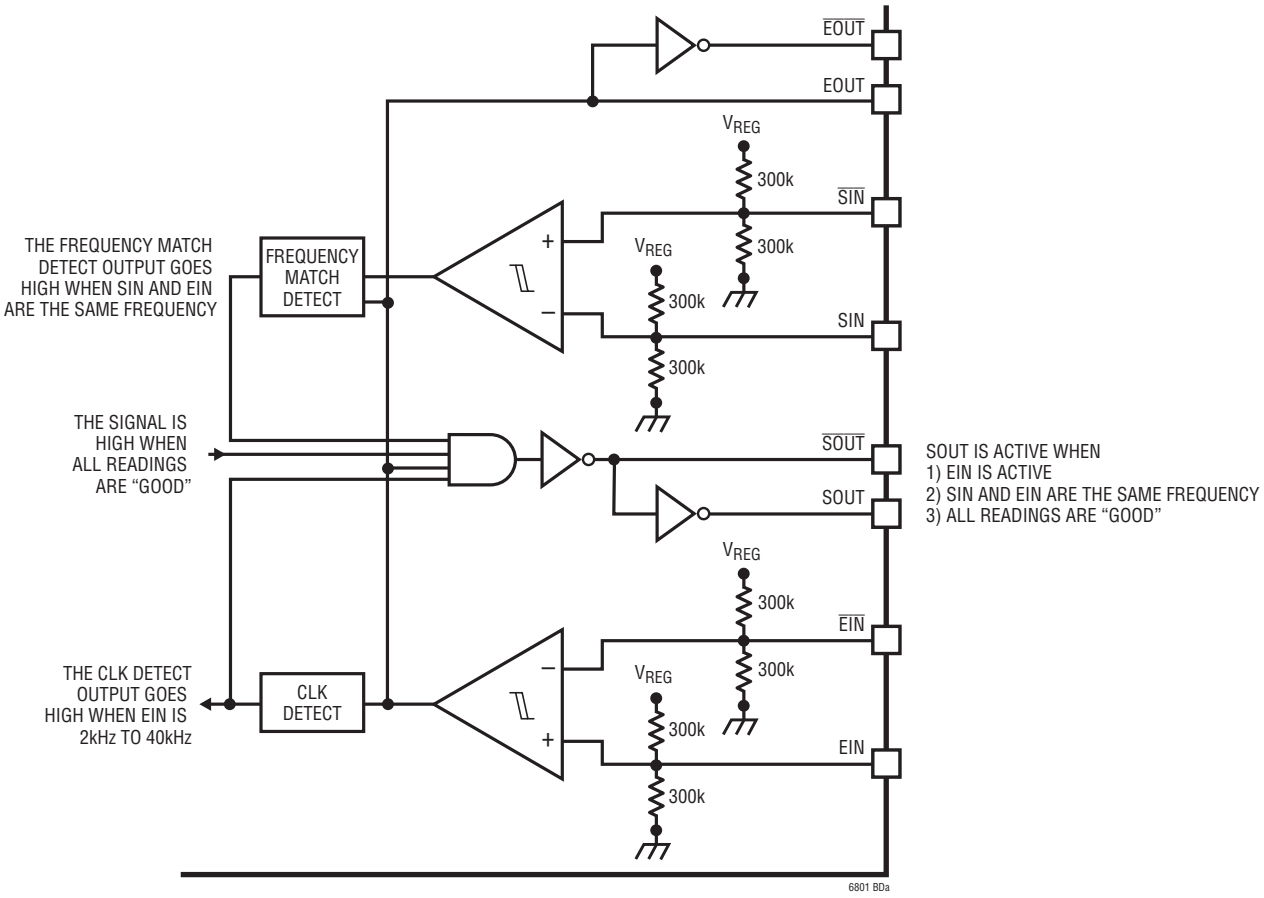
CC1	CC0	CELL COUNT
V_{REG}	V_{REG}	12
V_{REG}	V_{REF}	11
V_{REG}	V^-	10
V_{REF}	V_{REG}	9
V_{REF}	V_{REF}	8
V_{REF}	V^-	7
V^-	V_{REG}	6
V^-	V_{REF}	5
V^-	V^-	4

BLOCK DIAGRAM

The LTC6801 measures between 4 and 12 cell voltages and 2 temperature inputs. If all measurements are within an acceptable window, the LTC6801 will produce a differential clock output signal (SOUT, $\overline{SOUT}$). If any of the channels exceed user set upper and lower thresholds, a logic low signal is produced at SOUT.



BLOCK DIAGRAM OF ENABLE IN/OUT AND STATUS IN/OUT



APPLICATIONS INFORMATION

OVERVIEW

The LTC6801 is designed as an easy to implement, low-cost battery stack monitor that provides a simple indication of correct battery stack operation without requiring a microcontroller interface. For battery stack monitoring with cell voltage read back and discharge circuitry, refer to the LTC6802 battery stack monitor data sheet.

The LTC6801 contains a 12-bit ADC, a precision voltage reference, sampled comparator, high voltage multiplexer and timer/sequencer. During normal operation, the sequencer multiplexes the ADC inputs between each of the channel input pins in turn, performing a single comparison to the undervoltage and overvoltage thresholds. The V_{TEMP} inputs are also monitored for an undervoltage at a fixed threshold of $V_{REF}/2$.

The presence of a status output clock indicates the system is “OK”. Becase the status output is dynamic, it cannot get stuck in the “OK” state.

STACKED OPERATION

Each LTC6801 monitors a group of up to 12 series connected cells. Groups of cells can be connected in series or parallel to form a large battery pack. The LTC6801s can be daisychained with simple capacitive or transformer coupling. This allows every cell in a large battery pack to be monitored with a single signal. Figure 2 illustrates monitoring of 36 series connected cells.

To cancel systematic duty cycle distortion through the clock buffers, it is recommended that the clock lines are cross-coupled (EOUT goes to $\overline{EIN}$ etc.) as they route up and down the stack as shown in Figure 2.

INDEPENDENT OPERATION

Figure 3 shows how three groups of 12 cells can be monitored independently.

REGULATED OUTPUTS

A regulated voltage is provided at the V_{REG} pin, biased from the battery stack. The V_{REG} pin can supply up to 4mA at 5V and may be used to power small external circuits. The regulated output remains at 5V continually, as long as the total stack voltage is between 10V and 50V.

A low current, precision reference voltage is provided at the V_{REF} pin, which can drive loads of greater than 100k. The V_{REF} output is high impedance when the LTC6801 is idle.

Both the V_{REG} and V_{REF} pins must be bypassed to V^- with a 1µF capacitor.

CONTROL INPUTS

The LTC6801 thresholds are controlled by the UV1, UV0, OV1 and OV0 pins. These pins are designed to be tied directly to V_{REG}, V_{REF} or V^- in order to set the comparison thresholds for all channels simultaneously. The pins are not designed to be variable. In particular, changes made to the pins while the chip is not in idle mode may result in unpredictable behavior. See Tables 1 and 2 for setting and threshold information.

APPLICATIONS INFORMATION

ENABLE INPUTS

In order to support stacked operation, the LTC6801 is enabled through a differential signal chain encompassing the EIN/$\overline{\text{EIN}}$, EOUT/$\overline{\text{EOUT}}$, and SIN/$\overline{\text{SIN}}$ pins.

The LTC6801 will be enabled if a differential square wave with a frequency between 2kHz and 40kHz is applied at EIN/$\overline{\text{EIN}}$. Otherwise, the LTC6801 will default to a low power idle mode.

If the differential signal at SIN/$\overline{\text{SIN}}$ is not equal in frequency to the differential signal output at EOUT/$\overline{\text{EOUT}}$, the LTC6801 will be enabled but SOUT will be held at 0V and $\overline{\text{SOUT}}$ will be held at V_{REG}.

For the simplest operation in a single chip configuration, EOUT should be connected directly to SIN and $\overline{\text{EOUT}}$ should be connected directly to $\overline{\text{SIN}}$, and a square wave with a frequency between 2kHz and 40kHz should be applied differentially to EIN and $\overline{\text{EIN}}$. For enable clock frequencies up to 10kHz, a single-ended square wave with a 5V swing may be used at EIN while a 1nF capacitor is connected from $\overline{\text{EIN}}$ to V^-.

STATUS OUTPUT

If the chip is properly enabled (EIN/$\overline{\text{EIN}}$, SIN/$\overline{\text{SIN}}$ are the same frequency), all cells are within the undervoltage and overvoltage thresholds, and the voltage at V_{TEMP1} and V_{TEMP2} is over one half V_{REF}, the differential output at SOUT/$\overline{\text{SOUT}}$ will toggle at the same frequency and in phase with the signal at EIN/$\overline{\text{EIN}}$. Otherwise, SOUT will be low and $\overline{\text{SOUT}}$ will be high.

The maximum delay between when a bad cell voltage occurs and when it is detected depends on the measurement duty cycle setting. The SOUT clock turns on or off at the end of each measurement cycle. Figure 4 shows the maximum detection delay in continuous monitor mode (DC pin tied to V_{REG}).

FAULT PROTECTION

Overview

Care should always be taken when using high energy sources such as batteries. There are countless ways that systems can be [mis-]configured during the assembly and service procedures that can impact a battery's long term performance. Table 6 shows various situations to consider when planning protection circuitry.

Battery Interconnection Integrity

Please note: The last condition shown in the FMEA table could cause catastrophic IC failures. In this case, the battery string integrity is lost within a cell group monitored by an LTC6801. This condition could place excessive stress on certain cell input signal clamp-diodes and probably lead to IC failure. If this scenario seems at all likely in a particular application, series fuses and parallel Schottky diodes should be connected as shown in Figure 5 to limit stress on the IC inputs. The diodes used in this situation need current ratings sufficient to open the protective fuse in the battery tap signal.

APPLICATIONS INFORMATION

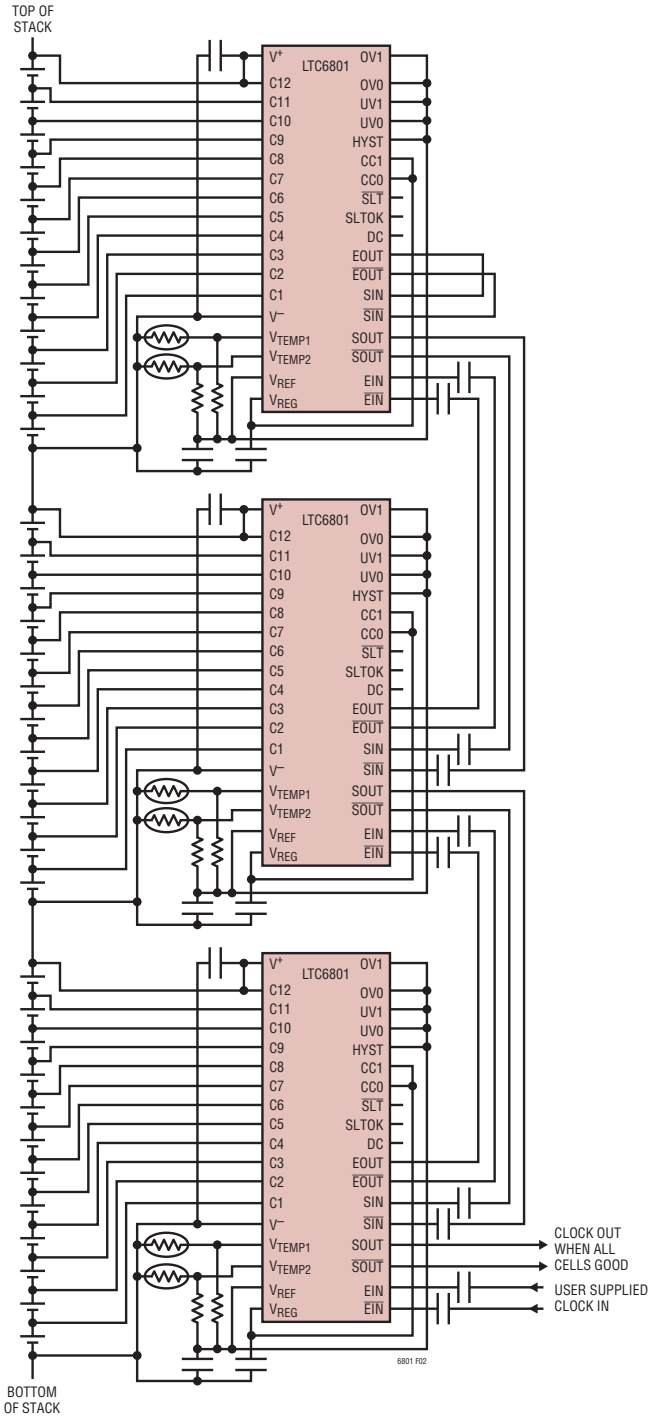


Figure 2. Serial Connection of Status Lines for Multiple 6801s on the Same PCB (Simplified Schematic, Not All Components Shown)

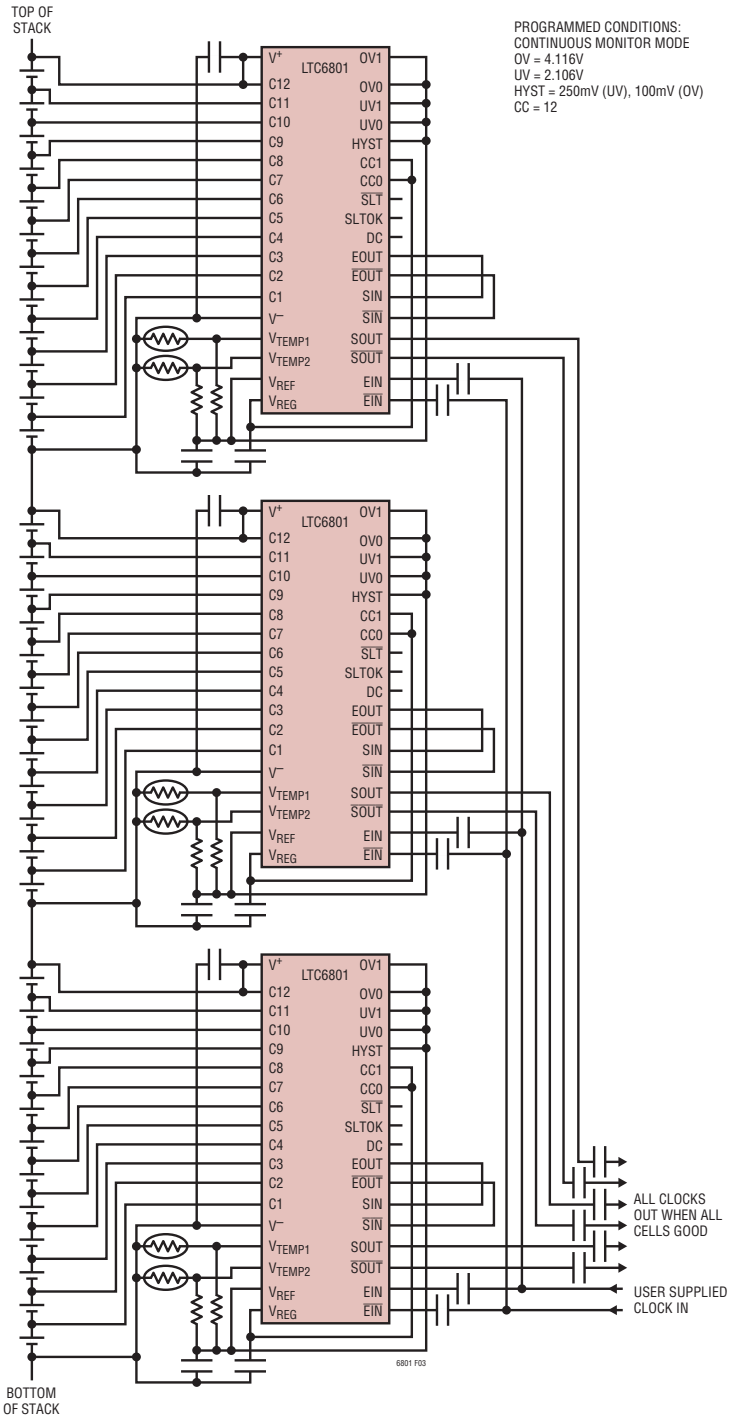


Figure 3. Independent Status Lines for Multiple 6801s on the Same PCB (Simplified Schematic, Not All Components Shown)

APPLICATIONS INFORMATION

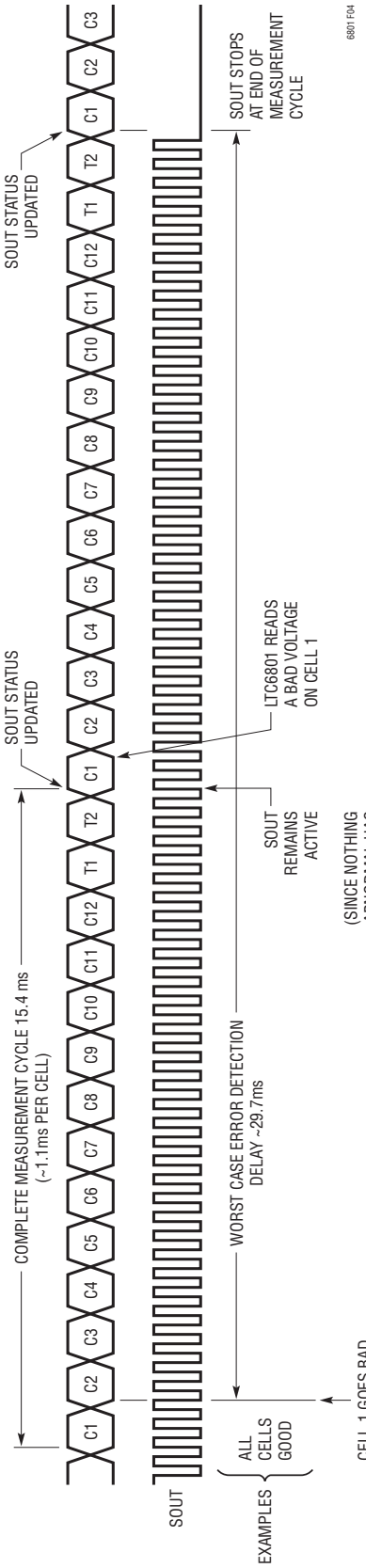


Figure 4. Cell UV/OV Detection Delay in Continuous Monitor Mode

APPLICATIONS INFORMATION

Table 6. Failure Mechanism Effect Analysis (FMEA)

SCENARIO	EFFECT	DESIGN MITIGATION
Cell input open-circuit (random)	Power-up sequence at IC inputs	Clamp diodes at each pin to V^+ & V^- (within IC) provide alternate PowerPath.
Cell input open-circuit (random)	Differential input voltage overstress	Zener diodes across each cell voltage input pair (within IC) limit stress.
Top cell input connection loss (V^+)	Power will come from highest connected cell input	Clamp diodes at each pin to V^+ and V^- (within IC) provide alternate PowerPath. Error condition will be indicated by all upstream and downstream units (no clock on SOUT/ $\overline{SOUT}$).
Bottom cell input connection loss (V^-)	Power will come from lowest connected cell input	Clamp diodes at each pin to V^+ and V^- (within IC) provide alternate PowerPath. Error condition will be indicated by all upstream and downstream units (no clock on SOUT/ $\overline{SOUT}$).
Power input disconnection (amongst stacked units)	Loss of supply connections	Clamp diodes at each pin to V^+ and V^- (within IC) provide alternate PowerPath. Error condition will be indicated by all upstream and downstream units (no clock on SOUT/ $\overline{SOUT}$).
Status link disconnection (between stacked units)	Break of “daisy chain” communication (no stress to ICs)	Daisy chain will be broken and error condition will be indicated by all upstream and downstream units (no clock on SOUT/ $\overline{SOUT}$).
Short between any two configuration inputs	Power supplies connected to pins will be shorted	If V_{REF} or V_{REG} is shorted to V^-, supply will be removed from internal circuitry and error condition will be indicated by all upstream and downstream units (no clock on SOUT/ $\overline{SOUT}$). If V_{REF} is shorted to V_{REG}, a self test error will be flagged.
Open connection on configuration input	Control input will be pulled towards positive or negative potential depending on pin	Control input will be pulled to a more stringent condition (larger number of channels, higher UV threshold, lower OV threshold, shorter duty cycle, etc. ensuring either more stringent monitoring or error condition will be indicated by all upstream and downstream units (no clock on SOUT/ $\overline{SOUT}$).
Cell-pack integrity, break between stacked units	Daisy-chain voltage reversal up to full stack potential	Full stack potential may appear across status/ enable isolation devices, but will not be seen by the IC. isolation capacitors should therefore be rated to withstand the full stack potential.
Cell-pack integrity, break within stacked unit	Cell input reverse overstress	Add battery tap fuses and Schottky diodes in parallel with the cell inputs to limit stress on IC. Diode and connections must handle current sufficient to open fuse

APPLICATIONS INFORMATION

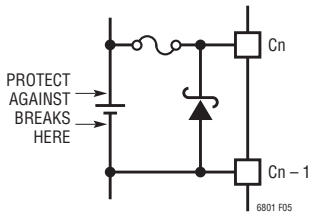


Figure 5. Using Fuses and Diodes for Cell Input Protection (One Cell Connection Shown)

Internal Protection Structure

The LTC6801 incorporates a number of protective structures, including parasitic diodes, Zener-like overvoltage suppressors, and other internal features that provide protection against ESD and certain overstress conditions that could arise in practice. Figure 6 shows a simplified internal schematic that indicates the significant protective structures and their connectivity. The various diodes indicate the approximate current versus voltage characteristics that are intrinsic to the part, which is useful in analyzing responses to certain external stresses, such as during a hot-start scenario.

SELF TEST CIRCUITRY

The LTC6801 has internal circuitry that performs a periodic self test of all measurement functions. The LTC6801 self test circuitry is intended to prevent undetectable failure modes. Accuracy and functionality of the voltage reference and comparator are verified, as well as functionality of the high voltage multiplexer and ADC decimation filter. Additionally, open connections on the cell input pins C1 to C11 are detected (Open connections on V^- or C12/V^+ will cause an undervoltage failure during the normal measurement cycle).

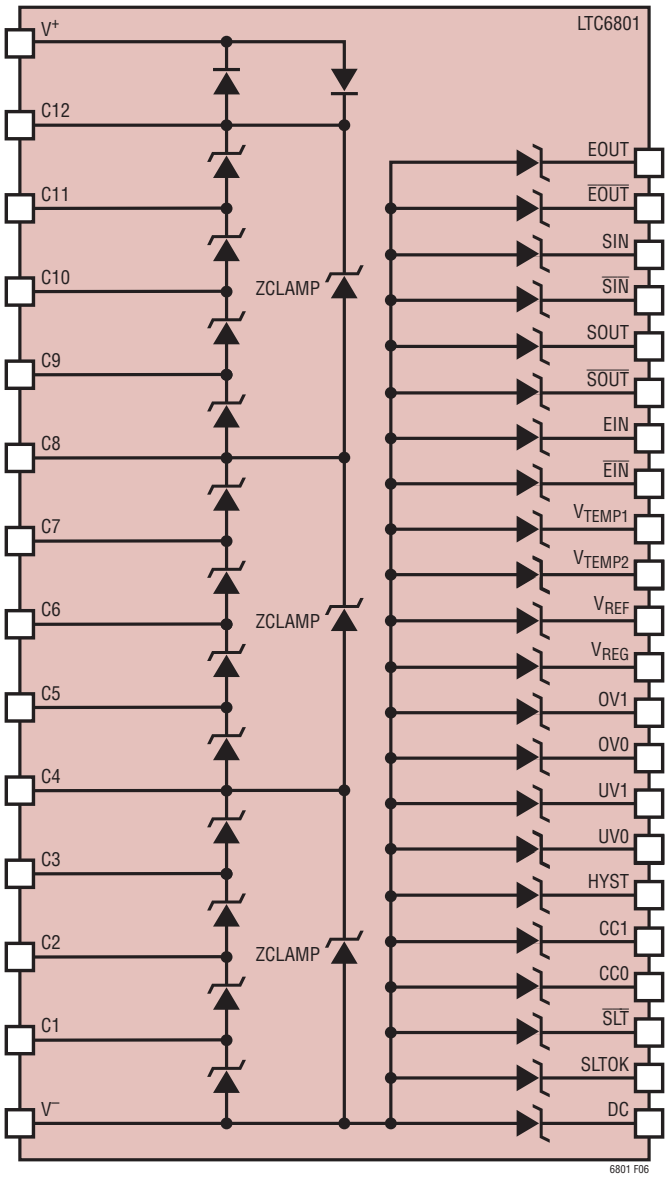


Figure 6. Internal Protection Structures

APPLICATIONS INFORMATION

Self Test Pins

The $\overline{SLT}$ pin is used to initiate a self test. It is configured as an open collector input/output. The pin should be normally tied to V_{REG} with a resistor greater than or equal to 100k or floated. The pin may be pulled low at any time to initiate a self test cycle.

The device will automatically initiate a self test if $\overline{SLT}$ has not been externally activated for 1024 measurement cycles, and pull down the $\overline{SLT}$ pin internally to indicate that it is in self test mode.

The SLTOK pin is a simple logic output. If the previous self test failed the output is held low, otherwise the output will be high. The SLTOK pin is high upon power-up. The SLTOK output can be connected to a microcontroller through an isolation path.

The LTC6801 status output will remain active while the SLTOK pin is low. The LTC6801 will continue to monitor cells if the self test fails. If the next self test passes, the SLTOK output returns high.

Reference and Comparator Verification

A secondary internal bandgap voltage reference (REF2) is included in the LTC6801 to aid in verification of the reference and comparator. During the self test cycle, the comparator and main reference are used to measure the REF2 voltage.

To verify the comparator functionality, the upper and lower thresholds are first set in a close window around the expected REF2 voltage and the comparator output is verified. Then the upper threshold is set below the REF2 voltage and the comparator output is verified again. Lastly, the lower threshold is set above the REF2 voltage and the comparator output is verified a third time.

The self test guarantees that V_{REF} is within 5% of the specified nominal value. Also, this test guarantees the analog portion of the ADC is working.

High Voltage Multiplexer Verification

The most dangerous failure mode of the high voltage multiplexer would be a stuck bit condition in the address decoder. Such a fault would cause some channels to be measured repeatedly while other channels are skipped. A skipped channel could mean a bad cell reading is not detectable. Other multiplexer failures, like the simultaneous selection of multiple channels, or shorts in the signal path, would result in an undervoltage or overvoltage condition on at least one of the channels.

The LTC6801 incorporates circuitry to ensure that all requested channels are measured during each measurement cycle and none are skipped. If a channel is skipped, an error is flagged during the self test cycle.

ADC Decimation Filter Verification

The ADC decimation filter test verifies that the digital circuits in the ADC are working, i.e. there are no stuck bits in the ADC output register. During each self test cycle, the LTC6801 feeds two test waveforms into the ADC. The internally generated waveforms were designed to generate complementary zebra patterns (alternating 0's and 1's) at the ADC output. If either of the waveforms generates an incorrect output value, an error is flagged during the self test cycle.

Open Cell Connection Detection

The open connection detection algorithm ensures that an open circuit is not misinterpreted as a valid cell reading.

APPLICATIONS INFORMATION

In the absence of external noise filtering, the input resistance of the ADC will cause open wires to produce a near zero reading. This reading will cause an undervoltage failure during the normal measurement cycle.

Some applications may include external noise filtering to improve the quality of the voltage comparisons. When an RC network is used to filter noise, an open wire may not produce a zero reading because the comparator input resistance is too large to discharge the capacitors on the input pin. Charge may build up on the open pin during successive measurement cycles to the extent that it could indicate a valid cell voltage reading.

During each self test cycle, the LTC6801 will sink 100µA to V^- from each side of the cell being measured. The undervoltage threshold is not checked during the self test because the 100µA pull-down current would cause false failures in some cases. If an input is open, this current will discharge any filtering capacitors and cause the input to float down to approximately 0.7V below the next lower cell input. In most cases, the cell voltage of the cell above the open input will exceed the overvoltage threshold and flag a self test error. During the normal measurement cycle, the LTC6801 will sink 1µA to V^- from each side of the cell being measured. If the cell voltages are low enough that an open wire is not detected as an overvoltage during self test, this current will cause the cell input to settle to a voltage low enough to trigger an undervoltage condition during the normal measurement cycle.

Note, an open cell connection may not be detected when the UV = 0.766V setting is used. For all other UV settings, an open cell connection will result in either a self test error or no SOUT clock.

Using The LTC6801 with Other Battery Monitors

When used in combination with an LTC6802-1, it is possible to check the LTC6801 self test result via the LTC6802-1 and its isolated SPI. As shown in Figure 7, the SLTOK output is tied to the GPIO2 pin on the LTC6802-1. SLTOK will remain high as long as it is passing the self test. A self test will occur automatically every 1024 measurement cycles (17 seconds to 9 minutes, depending on measurement duty cycle). A self test can be initiated by a falling edge on $\overline{SLT}$, via the LTC6802-1 GPIO1 line. A self test will start after the current measurement cycle is complete, and the SLTOK status will be valid when the self test completes. The worst case delay before SLTOK is valid in continuous monitor mode is approximately 15ms for the current cycle to complete plus 17ms for the self test to complete.

The 6802-1 can measure the LTC6801 reference, which will independently test the analog circuitry of the LTC6802.

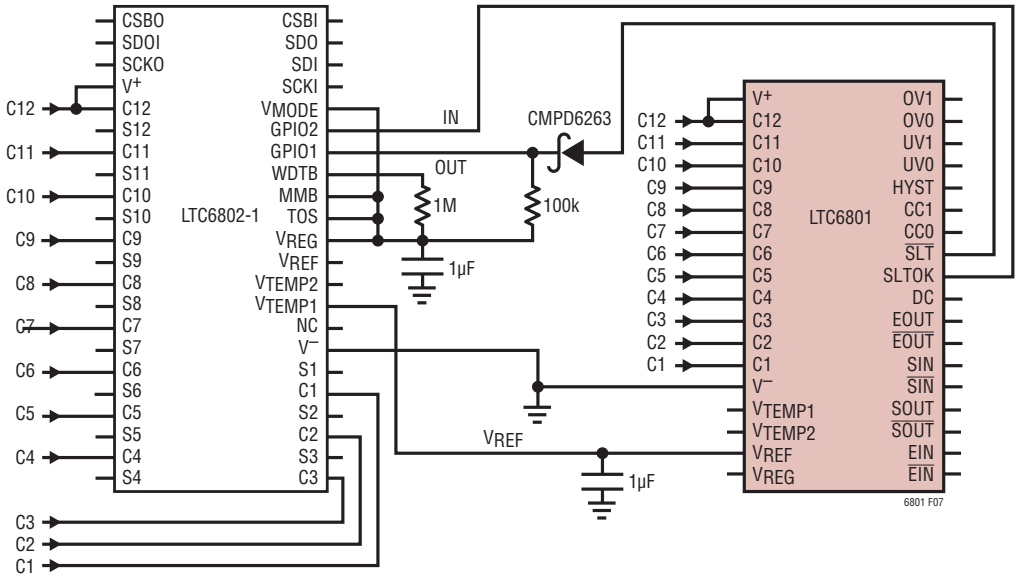


Figure 7. Interconnection of an LTC6802-1 and LTC6801 for Self Test.

APPLICATIONS INFORMATION

CELL-VOLTAGE FILTERING

The LTC6801 employs a sampling system to perform its analog-to-digital conversions and provides a conversion result that is essentially an average over the 0.5ms conversion window. If there is significant noise at frequencies near 500kHz there may be aliasing in the delta-sigma modulator. A lowpass filter with 30dB attenuation at 500kHz may be beneficial. Since the delta-sigma integration bandwidth is about 1kHz, the filter corner need not be lower than this to assure accurate conversions.

Series resistors of 1k may be inserted in the input paths without introducing measurement error. Shunt capacitors may be added from the cell inputs to V^-, creating RC filtering as shown in Figure 8. The combination of 1k and 10nF is recommended as a robust, cost effective noise filter.

MEASURING VARIOUS CELL COUNTS

The LTC6801 is designed to measure up to 12 cells depending on the state of the CC pins (See Table 5). When using an LTC6801 configured for measuring less than 12 cells, for instance choosing to measure 8 cells by tying both CC1 and CC0 to the V_{REF} pin, the highest cell potential (in this case C8) must be connected to the V^+ pin for proper operation. Unused cell connection pins (in this case C9 to C12) may be left floating or may also be tied to the highest cell potential.

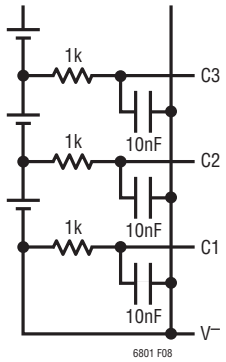


Figure 8. Adding RC Filtering to the Cell inputs

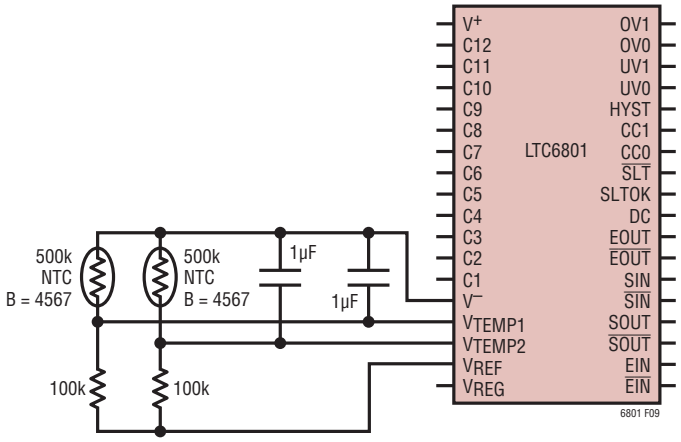


Figure 9. Driving Thermistors Directly from V_{REF}. Two Independent Probes With a +60°C Trip Point

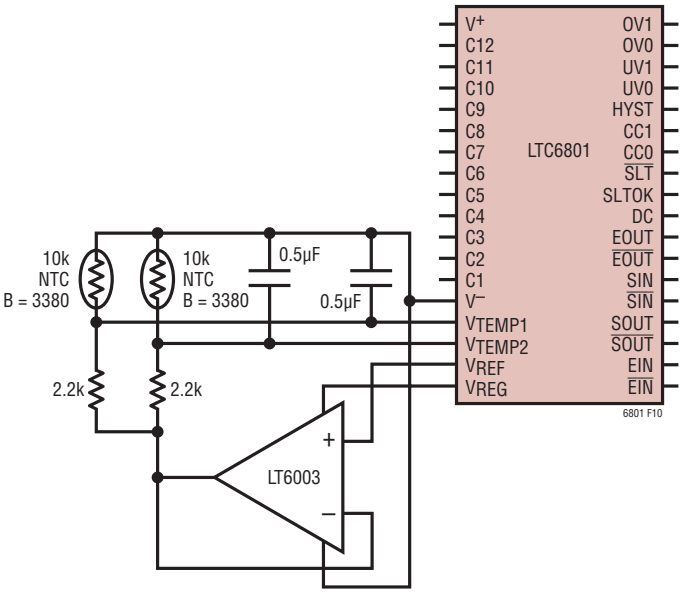


Figure 10. Buffering V_{REF} for Higher-Current Sensors. Two Independent Probes With a +70°C Trip Point

APPLICATIONS INFORMATION

READING EXTERNAL TEMPERATURE PROBES

The LTC6801 includes two channels of ADC input, V_{TEMP1} and V_{TEMP2}, that are intended to monitor thermistors (tempco about –4%/°C generally) or diodes (–2.2mV/°C typical) located within the cell array. Sensors can be powered directly from V_{REF} as shown in Figure 9 (up to 30µA typical).

The temperature measurement inputs (V_{TEMP1}, V_{TEMP2}) of the LTC6801 are comparator input channels with a voltage threshold of one-half V_{REF}. Input voltages above half V_{REF} are considered good. Voltages below the one-half V_{REF} threshold are considered a fault condition. The inputs may be used in combination with resistors, thermistors, or diodes to sense both an upper and lower temperature limit. Figure 9, Figure 10 and Figure 11 illustrate some possibilities. To ignore these inputs simply connect V_{TEMP1} and V_{TEMP2} to V_{REF}. A filtering capacitor to V^- is recommended to minimize the error caused by the approximately 700k input impedance of the ADC.

For sensors that require higher drive currents, a buffer amplifier may be used as shown in Figure 10. Power for the sensor is actually sourced indirectly from the V_{REG} pin in this case. Probe loads up to about 1mA maximum are supported in this configuration. Since V_{REF} is shut down while the LTC6801 is idle between measurement cycles, the thermistor drive is also shut off and thus power dissipation is minimized. Since V_{REG} remains always-on, the buffer op amp (LT6003 shown) is selected for its ultralow current consumption (10µA).

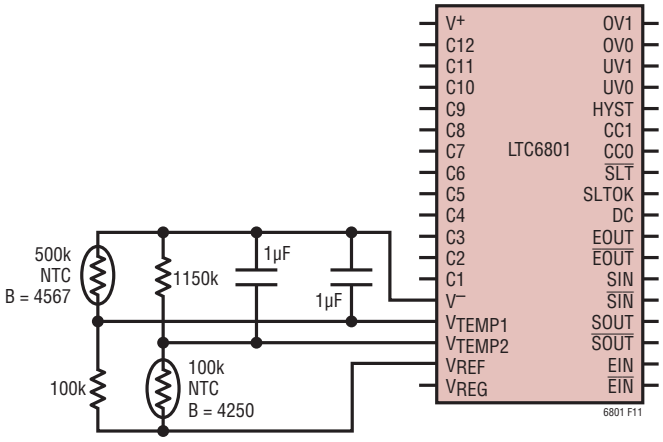


Figure 11. Sensing Both Upper and Lower Temperature Thresholds. This Example Monitors a –20°C to +60°C Window Detector. The Thermistors Should Be in Close Proximity

For circuits that include filtering capacitance, note that only the fastest DC setting (V_{REG} connection) will keep V_{REF} steady and allow the V_{TEMP} voltages to settle. To use the lower power DC settings, V_{REF} must be buffered (see Figure 10), so that a low impedance is presented to the ADC, with a time constant of no more than about 1ms.

ADVANTAGES OF DELTA-SIGMA ADCs

The LTC6801 employs a delta-sigma analog to digital converter for voltage measurement. The architecture of delta-sigma converters can vary considerably, but the common characteristic is that the input is sampled many times over the course of a conversion and then filtered or averaged to produce the digital output code.

APPLICATIONS INFORMATION

For a given sample rate, a delta-sigma converter can achieve excellent noise rejection while settling completely in a single conversion. This is particularly important for noisy automotive systems. Other advantages of delta-sigma converters are that they are inherently monotonic, meaning they have no missing codes, and they have excellent DC specifications.

The LTC6801's ADC has a second order delta-sigma modulator followed by a SINC2, finite impulse response (FIR) digital filter, with a lowpass bandwidth of 1kHz. The front-end sample rate is 512ksps, which greatly reduces input filtering requirements. A simple 16kHz, 1 pole filter composed of a 1k resistor and a 10nF capacitor at each input will provide adequate filtering for most applications. These component values will not degrade the DC accuracy of the ADC.

Each conversion consists of two phases – an autozero phase and a measurement phase. The ADC is autozeroed at each conversion, greatly improving CMRR.

USING TRANSFORMERS FOR GALVANIC ISOLATION

As shown in Figure 12, small gate-drive signal transformers can be used to interconnect devices and transport the enable and sense signals safely across an isolation barrier. Driving a transformer with a squarewave requires transient currents of several mA and frequency of operation at 20kHz or higher. Since the output pins of the LTC6801 are current limited at <1mA, a small external gate pair (NC7WZ17 dual buffer) is used to provide the needed drive current. 330Ω resistors are placed in series with each buffer output to optimize current flow into the transformer primary and a coupling capacitor provides prevention of current flow in static conditions. The secondary side is wired in a center-tapped configuration to terminate the common mode voltage and thus suppress noise pickup. The differential signal is terminated into 1500Ω to optimize the peak signal swing for the IC input (to about $\pm 4V_{P-P}$). Internal biasing features of the IC inputs maintain an optimal DC common mode level at the transformer secondary.

INTERCOMMUNICATION USING DATA ISOLATORS

As shown in Figure 13, an inexpensive and compact 2-channel data isolator is used to communicate the enable and the sense clocking signals between devices. The wiring carries isolator power and return plus two single-ended logic signals that are completely isolated at the upper device interface, so the signals are effectively differential from a common mode ingress perspective. The isolator provides excellent rejection of noise between battery groups, but consumes a few mA when operating, so a conventional opto-coupler and a few discretes provide a power-down scheme for periods where no monitoring is needed. Since the required current would load down V_{REG} if used directly, the NPN transistor is used to form a quasi-regulated 4.3V supply drawing from the full battery group potential, also moving significant thermal loading outside the IC. The PMOS FET is a low resistance switch controlled by the opto-coupler output. Since the opto-coupler is used to switch only a small current, the LED need only be driven with ~500µA. Powering down the bottom-of-stack isolator on the host µP side automatically powers down the entire isolator chain.

DEMO BOARD CIRCUIT

An LTC6801 demonstration circuit is shown in Figure 14. The circuit includes a 10kHz oscillator (U2) for the enable excitation and an LED (D15, driven by Q1) to indicate the state of the status outputs, plus an assortment of important protection components to ensure robust operation and hot-plugging of cell connections.

Series resistors (R14 to R21) provide a controlled coupling capacitor (C14 to C17) current in the inter-IC connections during startup or other abrupt potential changes, and associated clamp diodes (D13 and D14 quad array devices) redirect charge/surge current around the IC.

Input filters to each cell (R1, C1 to R12, C12) also use 6.2V Zener diodes (D1 to D12) to prevent overstress to the internal ESD clamps.

The V^+ input filter (R13, C13) has the same time constant as the ADC input filters so that the V^+ and C12 pins tend to track during start-up or transients, minimizing stress and ADC error.

APPLICATIONS INFORMATION

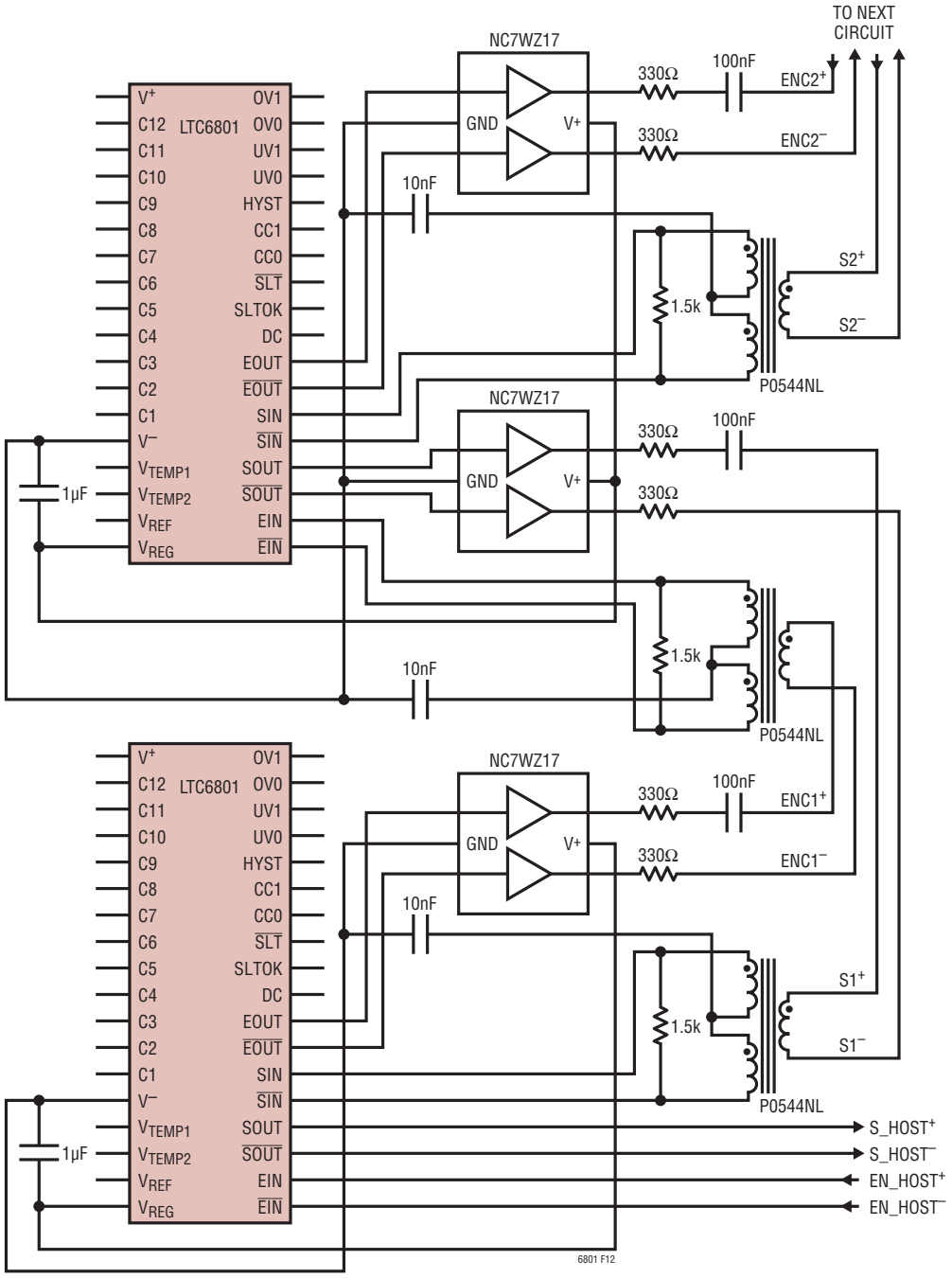


Figure 12. Using Transformers for Galvanic Isolation

APPLICATIONS INFORMATION

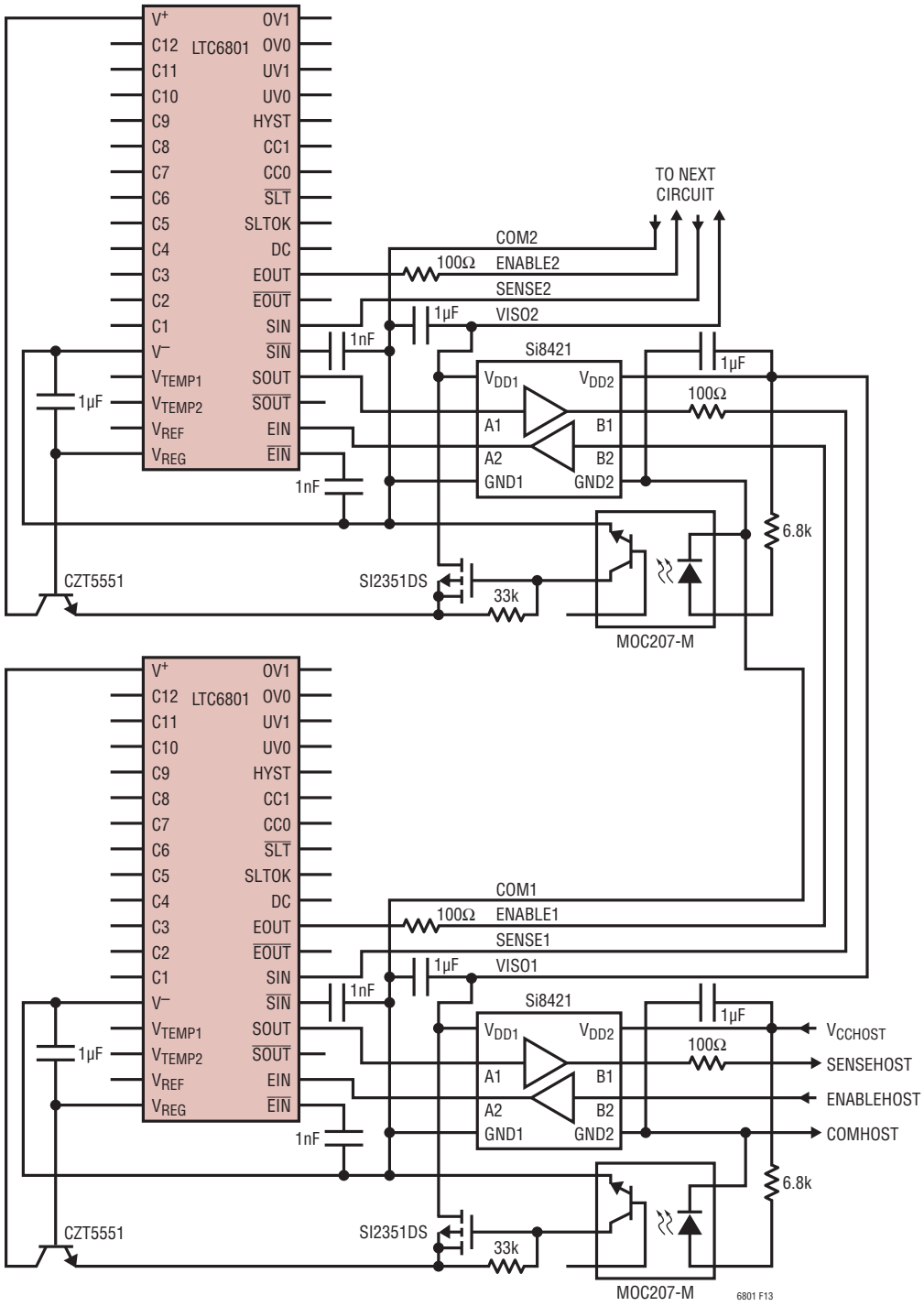


Figure 13. IC to IC Communication Using Data Isolators

APPLICATIONS INFORMATION

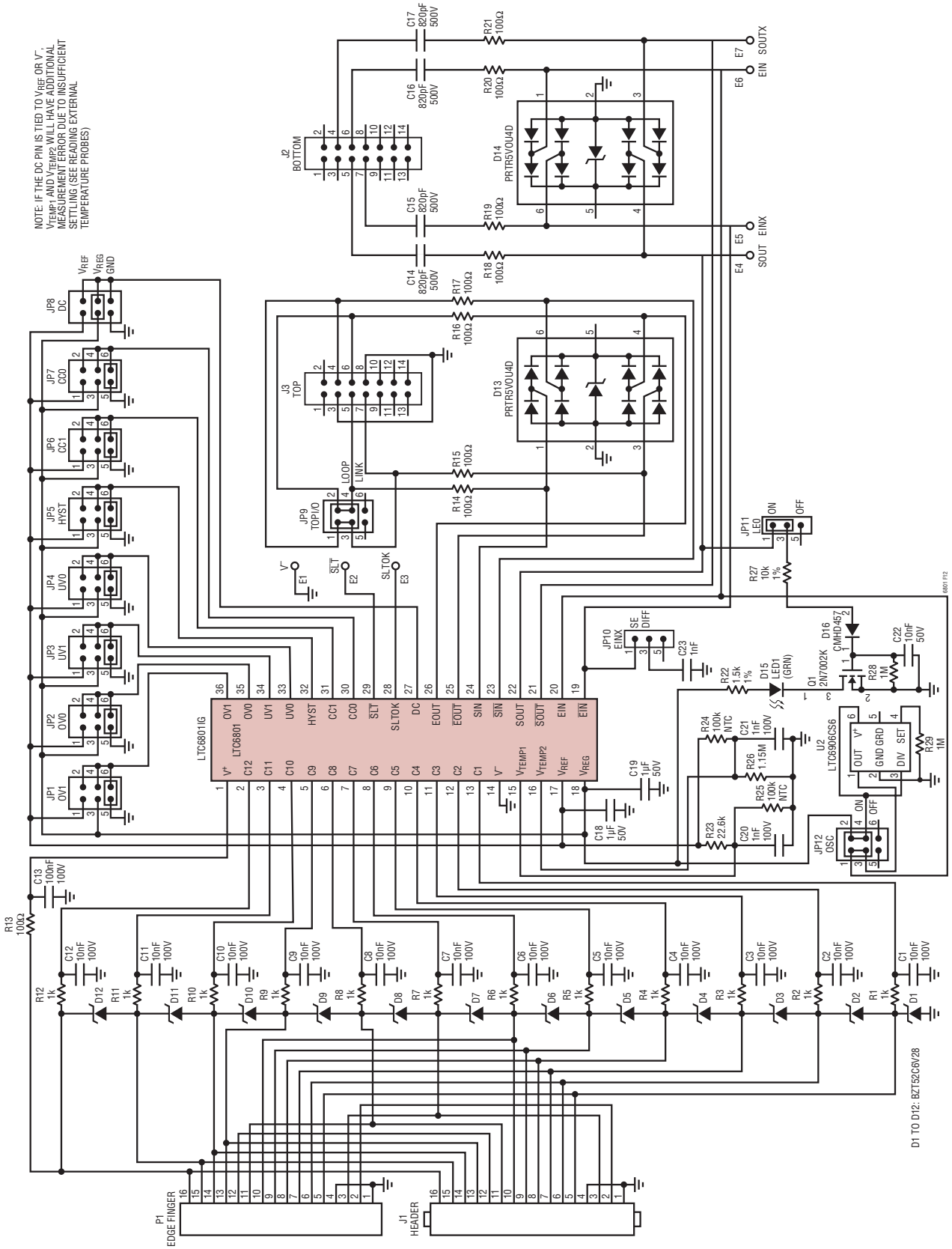
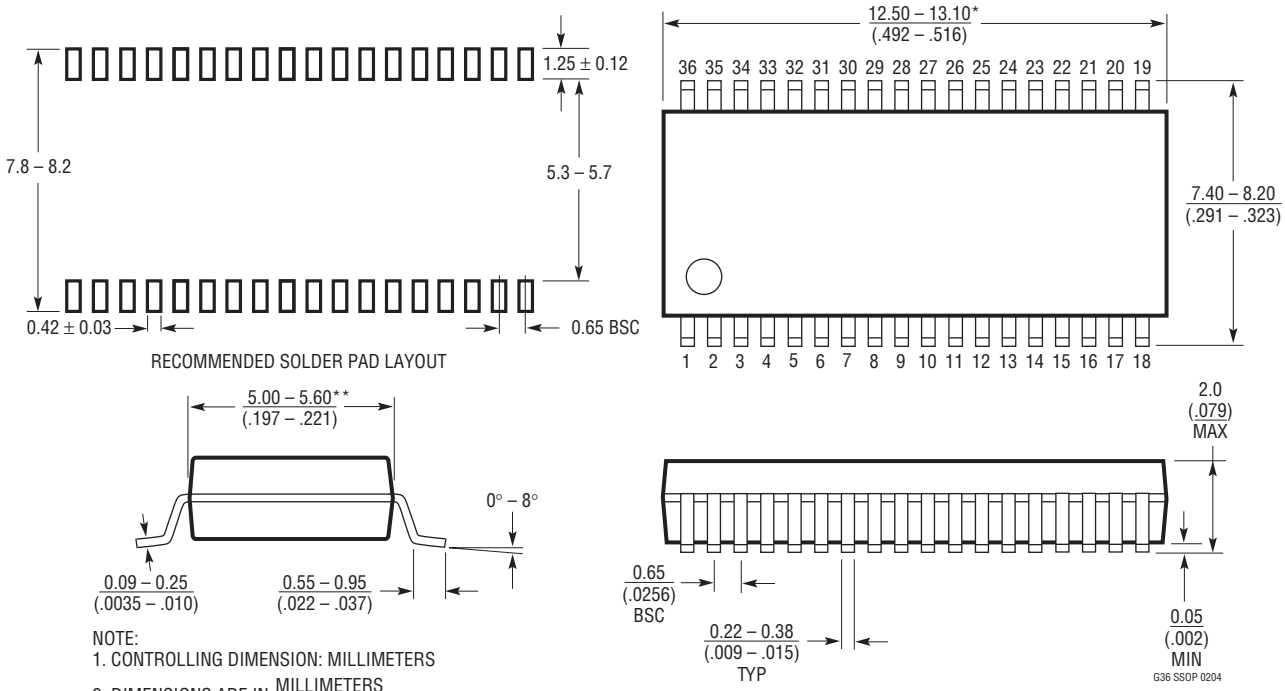


Figure 14. Schematic of LTC6801 Demo Circuit

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/10	H-grade part added. Reflected throughout the data sheet.	1 to 28
B	7/10	Updated V_{REG} Conditions. Updated Table 3	3 9

TYPICAL APPLICATION

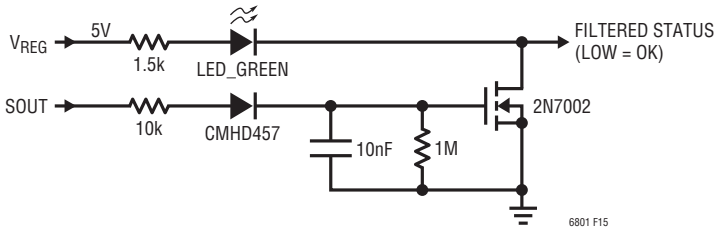


Figure 15. Alarm Qualification Filter/Status Indicator

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6802-1	Multi-Cell Battery Stack Monitor with a Stackable Serial Interface	Complete Battery Monitoring IC with 0.25% Cell Measurement Accuracy. Level-Shifting Serial Interface Allows Multiple LTC6802-1 Devices to be Daisy-Chained without Opto-Couplers or Isolators
LTC6802-2	Multi-Cell Battery Stack Monitor with an Individually Addressable Serial Interface	Functionally Equivalent to LTC6802-1: Parallel Connection Between Microcontroller and Multiple LTC6802-2 Devices

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