Quartus II Software Version 9.1 SP2 Device Support Release Notes

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus** directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

This document contains the following sections:

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Arria® II GX	EP2AGX95	EP2AGX125
	EP2AGX190	EP2AGX260
Cyclone IV E	EP4CE6	EP4CE10
	EP4CE15	EP4CE22
	EP4CE30	EP4CE40
	EP4CE55	EP4CE75
Cyclone IV GX	EP4CGX15	
Stratix IV	EP4SE230	EP4SE360
	EP4SE530	EP4SGX290
	EP4SGX360	EP4SGX530
	EP4S40G5	EP4S100G3
	EP4S100G4	EP4S100G5

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, the Compiler does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Cyclone III LS	EP3CLS70	EP3CLS100
Cyclone IV GX	EP4CGX22	EP4CGX30
Stratix IV	EP4SGX70	EP4SGX110
	EP4SGX530KF43	EP4SE820

Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices	
Cyclone IV GX	EP4CGX30CF23	EP4CGX50
	EP4CGX75	EP4CGX110
	EP4CGX150	

Compilation Support

Compilation support with preliminary timing and power analysis support is provided for the following HardCopy® III, HardCopy IV E, and HardCopy IV GX devices.

Devices with Compilation Support

Device Family	Devices	
HardCopy® III	HC325	HC335
HardCopy IV	HC4E25	HC4E35
	HC4GX15	HC4GX25
	HC4GX35	

Memory Requirements/Recommendations

A full installation of the Altera Complete Design Suite requires approximately 8.2 GB of available disk space on the drive or partition where you are installing the Altera Complete Design Suite and approximately 30 MB of available space on the drive that contains your **TEMP** directory (Windows only).

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of SOF files and the size and number of devices being configured.

Altera recommends that your system be configured to provide swap space (virtual memory) equal to the recommended physical RAM that is required to process your design.

The following table shows the memory required to process designs targeted for Altera devices.

Memory Requirements/Recommendations (Part 1 of 2)

Device	Recommended Physical RAM	
	32-bit	**64-bit**
Arria GX (EP1AGX20)	512 MB	512 MB
Cyclone (EP1C3, EP1C4, EP1C6, EP1C12, EP1C20)		
Cyclone II (EP2C5, EP2C8, EP2C20)		
Cyclone III (EP3C5, EP3C10, EP3C16, EP3C25, EP3C40)		
Cyclone IV E (EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40)		
Cyclone IV GX (EP4CGX15, EP4CGX22, EP4CGX30)		
All MAX® series and MAX II device families		
Stratix (EP1S10, EP1S20)		
Stratix GX (EP1SGX10)		
Stratix II (EP2S15)		
Cyclone III (EP3C55, EP3C80)	768 MB	1.0 GB
Cyclone IV E (EP4CE55, EP4CE75)		
Arria GX (EP1AGX35, EP1AGX50, EP1AGX60)	1.0 GB	1.5 GB
Arria II GX (EP2AGX45)		
Cyclone II (EP2C35, EP2C50)		
Cyclone IV E (EP4CE115)		
Cyclone IV GX (EP4CGX50, EP4CGX75)		
Stratix (EP1S25, EP1S30, EP1S40, EP1S60)		
Stratix GX (EP1SGX25, EP1SGX40)		
Stratix II (EP2S30)		
Stratix II GX (EP2SGX30, EP2SGX60)		
Stratix III (EP3SL50, EP3SE50, EP3SL70)		

Memory Requirements/Recommendations (Part 2 of 2)

Device	Recommended Physical RAM	
	32-bit	**64-bit**
Arria GX (EP1AGX90)	1.5 GB	2.0 GB
Arria II GX (EP2AGX65)		
Cyclone II (EP2C70)		
Cyclone III (EP3C120)		
Cyclone III LS (EP3CLS70, EP3CLS100)		
Cyclone IV GX (EP4CGX110, EP4CGX150)		
HardCopy II (HC210)		
Stratix (EP1S80)		
Stratix II (EP2S60, EP2S90)		
Stratix II GX (EP2SGX90)		
Stratix III (EP3SE80)		
Stratix IV (EP4SGX70)		
Arria II GX (EP2AGX95, EP2AGX125, EP2AGX190)	3.0 GB	4.0 GB
Cyclone III LS (EP3CLS150, EP3CLS200)		
Stratix II (EP2S130, EP2S180)		
Stratix II GX (EP2SGX130)		
HardCopy II (HC220, HC230, HC240)		
Stratix III (EP3SL110, EP3SE110, EP3SE150, EP3SL200)		
Stratix IV (EP4SGX110, EP4SGX230)		
Stratix IV GT (EP4S40G2 and EP4S100G2)		
Arria II GX (EP2AGX260)	4.0 GB	6.0 GB
Stratix III (EP3SE260, EP3SL340)		
Stratix IV (EP4SGX290)		
Stratix IV (EP4SGX360, EP4SGX530, EP4SE530)	N/A	8.0 GB
Stratix IV GT (EP4S40G5, EP4S100G3, EP4S100G4, and EP4S100G5)		
HardCopy III (HC3E25)		
HardCopy IV (HC4E25)		
Stratix IV (EP4SE820)	N/A	12.0 GB
HardCopy III (HC3E35)		
HardCopy IV (HC4GX15, HC4GX25. HC4GX35)		
HardCopy IV (HC4E35)	N/A	16.0 GB

Timing and Power Models

This section contains a summary of timing and power model status in the current version of the Quartus II software.

Devices with Timing and Power Models (Part 1 of 2)

Device Family	Device	Timing Model Status	Power Model Status
Arria GX	EP1AGX20	Final – 7.2	Final – 7.2
	EP1AGX35	Final – 7.2	
	EP1AGX50	Final – 7.2	
	EP1AGX60	Final – 7.2	
	EP1AGX90	Final – 7.2	
Aria II GX	EP2AGX45	Preliminary	Preliminary
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190		
	EP2AGX260		
Cyclone III	EP3C5	Final – 8.0 SP1	Final – 8.1
	EP3C10	Final – 8.0 SP1	
	EP3C16	Final – 8.0 SP1	
	EP3C25	Final – 7.2 SP1	
	EP3C40	Final – 8.0	
	EP3C55	Final – 8.0	
	EP3C80	Final – 8.0	
	EP3C120	Final – 7.2 SP1	
Cyclone III LS	EPC3LS70	Preliminary	Preliminary
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	(All)	Preliminary	Preliminary
Cyclone IV GX	(All)	Preliminary	Preliminary
HardCopy II	HC210	Correlated – 8.0	Correlated – 7.2
	HC210W		
	HC220		
	HC230		
	HC240		
HardCopy III	(All)	Preliminary	Preliminary
HardCopy IV E	(All)	Preliminary	Preliminary
HardCopy IV GX		Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		

Devices with Timing and Power Models (Part 2 of 2)

Device Family	Device	Timing Model Status	Power Model Status
Stratix II GX	EP2SGX30	Final – 7.0	Final – 7.1
	EP2SGX60	Final – 7.0	
	EP2SGX90	Final – 6.1	
	EP2SGX130	Final – 6.1	
Stratix III	EP3SE50	Final – 9.0	Final – 9.0
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Final – 9.0	
	EP3SL50	Final – 9.0	
	EP3SL70	Final – 9.0	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Final – 9.0	
	EP3SL340	Final – 8.1	
Stratix IV	EP4SE230	Final – 9.1 SP1	Preliminary
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2	
	EP4SE530		
	EP4SE820	Preliminary	
	EP4SGX70		
	EP4SGX110		
	EP4SGX290	Final – 9.1 SP2	
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4		
	EP4S100G5		

The current version of the Quartus II software also includes final timing models for the Cyclone, Cyclone II, MAX, MAX II, Stratix, Stratix II, and Stratix GX device families. Timing models for these device families became final in the Quartus II software versions 6.0 and earlier.

The current version of the Quartus II software also includes final power models for the Cyclone, Cyclone II, MAX, MAX II, Stratix, Stratix II, and Stratix GX device families. Power models for these device families became final in the Quartus II software versions 6.0 and earlier.

Changes in Device Support

Cyclone IV GX incorrect simulation

For Cyclone IV GX devices, when simulating a design containing an ALTLVDS megafunction, an incorrect reslt may occur when the **Enable bitslip control** option is enabled.

Applies to: Cyclone IV GX devices

Cyclone III automotive grade devices removed

Support for Cyclone III automotive grade devices has been removed for the Quartus II software version 9.1 SP2. Altera recommends Cyclone IV E automotive grade devices for new designs.

Applies to: Cyclone III devices

Stratix IV and HardCopy migration flow consistency

Stratix IV device EP4SGX530KH50C3 and HardCopy IV device HC4GX35FF have different numbers of PCIE HIP blocks, which causes an inconsistent migration flow. This issue has been fixed in the Quartus II version 9.1 SP2 software.

Applies to: Stratix IV and HardCopy devices

Arria II GX transceiver limits differ

Arria II GX transceiver limits differ from the documented limits for the Quartus II software version 9.1 SP1 and SP2. Refer to the Arria II GX data sheet for the correct range.

Applies to: Arria II GX devices

Stratix III Corner PLL delay setting change

Stratix III devices EP3SE260 and EP3SL200 corner PLL delay settings are updated in the Quartus II version 9.1 SP2 software. This change improves the LVDS sampling performance for some applications.

Applies to: Stratix III devices

Stratix IV ATX PLL support

The Quartus II software version 9.1 SP2 incorrectly allows a design with an ATX PLL to successfully compile when the design is targeted for a Stratix IV device that does not support the ATX PLL. Consult the data sheet for availability of the ATX PLL.

Applies to: Stratix IV devices

Stratix II devices fail to configure with EPCS devices

Stratix II devices failed to configure properly vwith EPCS devices due to incorrect configuration length count used by the Quartus II 9.1 SP1 software. This issue is fixed in the Quartus II 9.1 SP2 software. To correct the problem, regenerate the programming file (**.pof**, **.rbf**) with the Quartus II 9.1 SP2 software or later. The **.sof** file is not affected.

Applies to: Stratix II devices

Cyclone IV GX devices enforce incorrect data rate

The Quartus II software version 9.1 SP1 enforces the incorrect transceiver data rate limits for Cyclone IV GX devices with C8 speed grade packages and all F324 or smaller packages. This issue is fixed in the Quartus II 9.1 SP2 software.

Applies to: Cyclone IV GX devices

VCCIO pin count incorrect with device migration turned ON

When you migrate from a Stratix IV to a HardCopy IV or HardCopy IV GX device, if a pin is NC in the Stratix IV device and VCCIO in either HardCopy device, the migration result is NC. The correct migration result should be VCCIO, when the referred I/O bank is available in all devices of the current migration chain.

Applies to: HardCopy IV and HardCopy IV GX devices

Arria II GX and Stratix IV GX require regenerating transceiver reconfiguration Memory Initialization File

When the transceiver channel and PLL dynamic reconfiguration is enabled, and the transceiver bonding mode is X4 or X8, the TX clock (`coreclkout`) is inactive after reconfiguration. You must regenerate the transceiver reconfiguration Memory Initialization File (**.mif**) with the Quartus II software version 9.1 SP1.

Applies to: Arria II GX and Stratix IV GX devices

Arria II GX designs require recompilation

The Quartus II software versions 9.1 and earlier can produce functional failures in Arria II GX designs due to race conditions in the secondary signal region of RAM. This possible malfunction is fixed in Quartus II software version 9.1 SP1, and requires that you recompile your design.

Applies to: Arria II GX devices

No vertical migration for Engineering Sample Stratix IV 230 GX and E and 530 GX and E

Stratix IV 230 GX and E and 530 GX and E devices in Engineering Sample version are not allowed for vertical migration with the production devices due to the voltage changes. (Core voltage for ES devices is 0.95V, while core voltage for production devices is 0.9V.). To access vertical migration, use the corresponding production device in the design.

Applies to: Stratix IV devices

Migration combinations of devices show fewer VCCIO pins

In certain migration combinations of Arria II GX and Stratix IV GX and Stratix E devices, fewer VCCIO pins may be seen as available, when vertical migration in the following paths is enabled. Recompile your design with the Quartus II software version 9.1 SP2.

Arria II GX devices

EP2AGX95EF35 with EP2AGX190FF35 or EP2AGX260FF35

EP2AGX125EF35 with EP2AGX190FF35 or EP2AGX260FF35

Pins AJ8 and G8 from VCCIO4B (bank 4B) turn to NC when migration is on in these combinations.

Stratix IV E devices

EP4SE530F43 with EP4SE820F43

Multiple VCCIO pins from banks 1B, 1C, 2B, 2C, 3C, 4C, 5B, 5C, 6B, 6C, 7C, 8C turn to NC, when migration is on.

Stratix IV GX devices

EP4SGX110FF35 with EP4SGX180FF35, EP4SGX230FF35, EP4SGX290FF35, EP4SGX360FF35, or HC4GX25LF1152 (HardCopy IV)

Multiple VCCIO pins from banks 1A, 1C, 3C, 4C, 6A, 6C, 7C, 8C turn to NC, when migration is on.

Applies to: Arria II GX and Stratix IV GX and E devices

Power down settings ignored

The **VCCHIP_R power** and **VCCHIP_L power** options have been removed from the Quartus II software in version 9.1 SP1. The **Opportunistically power off** setting is no longer available; use the **Power on** setting instead.

Applies to: Stratix IV GX and Stratix IV GT devices

Design software support for mature device families

Design software support for FLEX, APEX, ACEX, and HardCopy Stratix device families is not provided in versions of the Quartus II software beginning with version 9.1. Use the Quartus II software version 9.0 or earlier to support those devices. The Quartus II software version 9.0 and the associated service packs will remain available on the Altera website (**http://www.altera.com**).

Applies to: ACEX, APEX, FLEX and HardCopy Stratix device families